LONWORKS®

LPT-11 Link Power Transceiver

User's Guide

Version 1

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Corporation

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Introduction

The LPT-11 Link Power Twisted Pair Transceiver provides a simple, cost effective method of adding a network-powered LONWORKS transceiver to any Neuron® Chip-based sensor, activator, display, lighting device, or general purpose I/O controller. The LPT-11 transceiver consists of a Single In-Line Package (SIP) containing a 78kbps differential Manchester coded communication transceiver, a switching power supply that draws power from the twisted pair network, and connections for the Neuron Chip Communications Port (CP) lines and the twisted pair network. The LPT-11 transceiver eliminates the need to use a local power supply for each device, since device power is supplied by a central power supply over the same twisted wire pair that handles network communications. Up to 128 devices can be supported on a single free topology network segment.

The LPT-11 transceiver supports free topology wiring, freeing the system installer from the need to wire in a doubly-terminated bus arrangement. Star, bus, and loop wiring are all supported by this architecture. Free topology wiring reduces the time and expense of system installation by allowing the wiring to be installed in the most expeditious manner. It also simplifies network expansion by alleviating the need for the installer to follow strict rules about stub lengths. Should it be necessary to add more devices or wire in excess of the system limits, then two or more link power systems can be interconnected with an inexpensive, physical layer repeater. The LPT-11 contains built-in circuitry to allow connection to one or more FTT-10A transceivers back-to-back to make a repeater. The LPT-11 transceiver includes an integral switching power supply that can furnish +5VDC at up to 100mA. The LPT-11 transceiver derives its power directly from the switching power supply, leaving up to 100mA of current for a Neuron Chip, application electronics, sensors, actuators, and displays. The high current capability of the LPT-11 transceiver eliminates the need for local power supplies at each device, resulting in equipment and labor cost savings.

The LPT-11 transceiver is compatible with Echelon's FTT-10A Free Topology Transceiver and FT 3120®/FT 3150® Smart Transceivers (referred to hereafter as FT 31xx devices), and these transceivers can communicate with each other on a single twisted pair cable. This capability provides an inexpensive means of interfacing to devices whose current and/or voltage requirements would otherwise exceed the capacity of the link power segment. When equipped with an FTT-10A or FT 31xx transceiver, these devices can be operated from a local power supply without the need for additional electrical isolation from the link power network.

Using the LPT-11 transceiver can save literally thousands of hours of development time compared with a custom-designed transceiver. The LPT-11 transceiver is designed to comply with FCC, CE, ICES-003, CISPR22, EN55022, EN55024, and EN61000-4 EMC requirements, minimizing time consuming and expensive laboratory transceiver testing. As a UL, cUL, and TuV recognized component, the LPT-11 transceiver can be integrated into a product with minimal additional safety testing of the LPT-11 transceiver module. The LPT-11 transceiver also meets LONMARK® interoperability standards.

Applications

A conventional control system using bus topology wiring (such as RS-485) consists of a network of sensors and control outputs that are interconnected using a shielded twisted pair wire. In accordance with EIA RS-485 guidelines, all of the devices must be wired in a bus topology to limit electrical reflections and ensure reliable communications. There is a high cost associated with installing and maintaining the cable plant that links together the many elements of an RS-485-based control system. Bus topology wiring is more time consuming and expensive to install because the installer is unable to branch or star the wiring where convenient; all devices must be connected directly to the main bus. The installation of local power supplies for each device is especially expensive since it usually involves an AC mains connection.

Installing separate data and power wiring also implies that a technician's time will be spent troubleshooting the wiring harness to isolate and repair cable faults. Moreover, each time a sensor is added or an actuator is moved, both data and power wiring must be changed accordingly, often resulting in network down time until the new connections can be established.

The best solution for reducing installation and maintenance costs and simplifying system modifications is a free topology communication system that combines power and data on a common twisted wire pair. Echelon's link power technology offers just such a solution, and provides an elegant and inexpensive method of interconnecting the different elements of a distributed control system.

The link power system sends power and data on a common twisted wire pair, and allows the user to wire the control devices with virtually no topology restrictions. Power is supplied by a customer-furnished nominal 48VDC power supply, and flows through an LPI-10 Power Supply Interface onto the twisted pair wire (figure 1.1). The LPI-10 module isolates the power supply from wiring faults on the twisted pair, couples power to the system wiring, and terminates the twisted pair network.

There are two versions of the LPI-10 interface: a simple, low-cost, inductor-based design intended for customers who are building power supplies, and an electronic LPI-10 interface designed for use with off-the-shelf 48VDC power supplies.

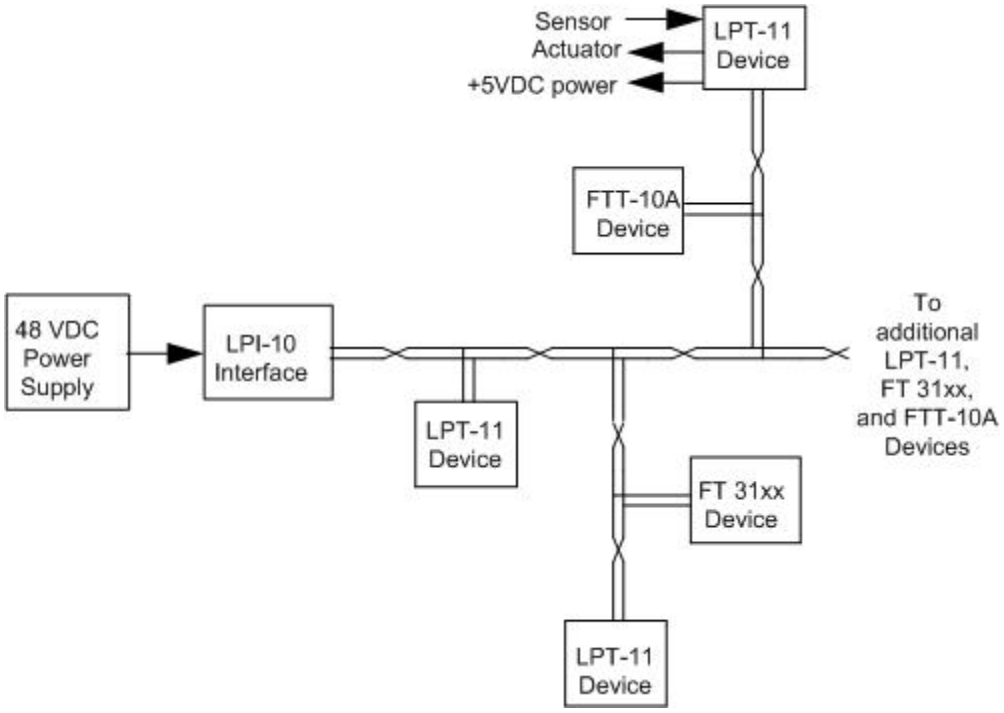

Figure 1.1 Free Topology Link Power System Example

LPT-11 Link Power Transceivers located along the twisted wire pair include integral switching power supplies. These supplies regulate the voltage on the twisted pair down to +5VDC at currents up to 100mA for use by the Neuron Chip and the various sensors, actuators, and displays. If a high current or high voltage device must be controlled, then the +5VDC power can be used to trigger an isolating high current triac, relay, or contactor.

The integral power supply does away with the need for a local AC-to-DC power supply, charging circuit, battery, and the related installation and labor expenses. The savings in money and time that results from eliminating the local power supply can be up to 20% of the total system cost; the larger the system, the greater the savings. Moreover, if standby batteries are used, then additional savings will be realized throughout the life of the system, since only one set of batteries will require service.

The link power system uses a single point of ground, at the LPI-10 module, and all of the LPT-11 transceivers electrically float relative to the local ground. Differential transmission minimizes the effects of common mode noise on signal transmission. If grounded sensors or actuators are used, then either the communication port (CP) or the I/O lines of the Neuron Chip must be electrically isolated.

Unlike bus wiring designs, the link power system uses a wiring scheme that supports star, loop, and/or bus wiring (figure 1.2). This design has many advantages:

1. The installer is free to select the method of wiring that best suits the installation, reducing the need for advanced planning and allowing last minute changes at the installation site.

2 If installers have been trained to use one style of wiring for all installations, free topology technology can be introduced without requiring retraining.
3. Retrofit installations with existing wiring plants can be accommodated with minimal rewiring, if any. This capability ensures that FT 3120 and FT 3150 Smart Transceiver technology can be adapted to both old and new projects.
4. Free topology permits FT 3120 and FT 3150 Smart Transceiver systems to be expanded in the future by simply tapping into the existing wiring where it is most convenient to do so. This reduces the time and expense of system expansion, and from the customer's perspective, keeps down the life cycle cost of the free topology network. See Chapter 5, *Network Cabling and Performance*, for a presentation of the five different network topologies.

System expansion is simplified in another important way, too. Each link power transciever incorporates a repeater function. If a link power system grows beyond the maximum number of transceivers or total wire distance, then additional link power systems can be added by interconnecting transceivers using the repeater function. The repeaters will transfer LonTalk® packets between the two systems, doubling the number of transceivers as well as the length of wire over which they communicate. The repeater function permits a link power system to grow as system needs expand, without retrofitting existing controllers or requiring the use of specialized bridges. Note that systems requiring high levels of network traffic may benefit from the use of LONWORKS routers which forward packets only when necessary. See Appendix A for more details.

Audience

This user guide is for developers of Link Power Transceiver-based LONWORKS devices and systems.

Content

This manual provides detailed technical specifications on the electrical and mechanical interfaces and operating environment characteristics for the LPT-11 transceiver module.

This document also provides guidelines for migrating applications from a LonBuilder® Developer's Workbench Emulator or NodeBuilder® Developer's Tool to a transceiver module-based product design. Vendor sources are included to simplify the task of integrating the transceiver module with application electronics.

Related Documentation

The following Echelon documents are suggested reading:

LonBuilder User's Guide (078-0001-01)

*NodeBuilder User's Guide (*078-0141-01*)*

Neuron C Programmer's Guide (078-0002-01)

LonBuilder Startup and Hardware Guide (078-0003-01)

LONWORKS LPI-10 Link Power Interface Module User's Guide (078-0104-01)

LONWORKS FTT-10A Free Topology Transceiver User's Guide (078-0156-01)

FT 3120/FT 3150 Smart Transceiver Data Book (005-0139-01)

LONWORKS Product Catalog (Catalog/Spring02)

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Electrical Interface

The LPT-11 Link Power Transceiver's 14 pins provide a polarity insensitive connection to the twisted pair network, an interface to the Neuron Chip communications port, and a switching power supply.

LPT-11 Pinout

The pinout of the LPT-11 transceiver is shown in table 2.1. The interconnection between the LPT-11 and a Neuron Chip is shown in the block diagram in figure 2.1. See figure 3.1 for the physical location of pin 1.

Table 2.1 LPT-11 Transceiver Pinout

Name	***Pin#***	***Function***
NET_A	1	Connection to TP network, polarity insensitive
NET_B	2	Connection to TP network, polarity insensitive
V+	3	Power supply input voltage (≈ 35VDC)
INDUCTOR	4	Power supply inductor connection
V_{CC}	5	+5VDC power output
GND	6	Power supply ground
CLK	7	Transceiver clock input from Neuron Chip
NC	8	No Connect (not connected internally)
TXD	9	Neuron Chip CP1
RXD	10	Neuron Chip CP0
NC	11	No Connect (not connected internally)
NC	12	No Connect (not connected internally)
NC	13	No Connect (not connected internally)
NC	14	No Connect (not connected internally)

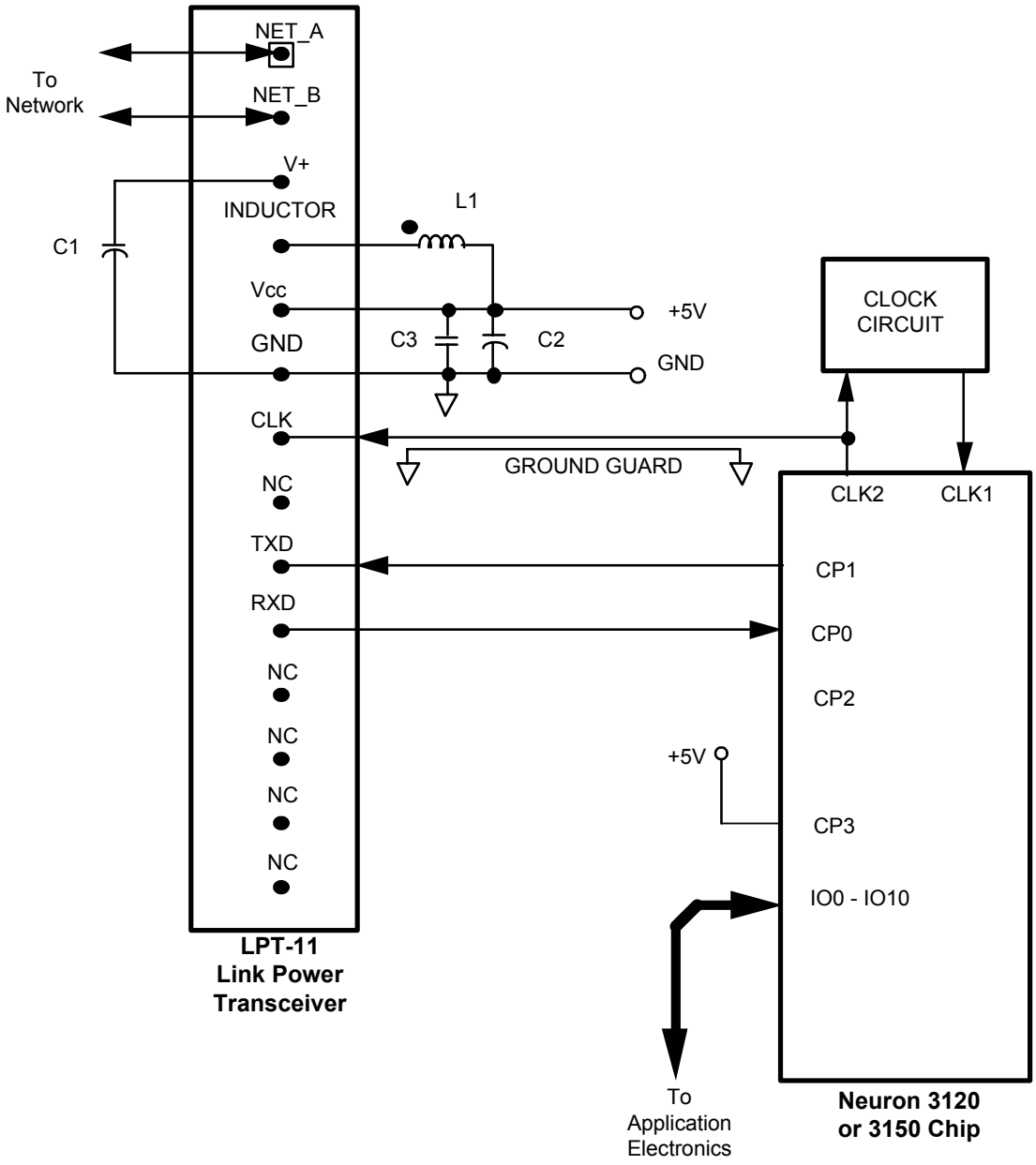

Figure 2.1 LPT-11 Transceiver-to-Neuron Chip Interconnections

Network Connection

The network connection (NET_A and NET_B) is polarity insensitive, and therefore either of the two twisted pair wires can be connected to either of the two NET pins. Details on network wiring are discussed in Chapter 5.

Transient protection may be required to protect the LPT-11 transceiver against surge voltages resulting from network transients and lightning strikes. Details on surge protection are discussed in Chapter 6.

Clock Input

The LPT-11 transceiver receives its clock input from the Neuron Chip via the CMOS input CLK pin. This pin is driven by the CLK2 output of the Neuron Chip, whether the Neuron Chip's oscillator or an external clock oscillator is used. Clock traces should be kept short (≤2cm) to minimize noise coupling.

The LPT-11 transceiver can operate at 20, 10, 5, or 2.5MHz. Operation at 2.5MHz does not comply with LONMARK interoperability guidelines for the TP/FT-10 channel. 1.25 MHz operation is not supported. The operating frequency is automatically detected on the CLK pin.

Neuron Chip Communications Port (CP) Lines

The LPT-11 transceiver transmits and receives LonTalk® network packets via the Neuron Chip's direct, single-ended mode over CP0-1. CP0 is the data input to the Neuron Chip and is connected to the LPT-11 transceiver's RXD pin. CP1 is the data output from the Neuron Chip and is connected to the TXD pin. These connections are summarized in table 2.2.

Table 2.2 Neuron Chip CP Line Connections

Neuron Chip Pin	*Neuron Chip Function*	*LPT-11 Pin*
CP0	Data input	RXD
CP1	Data output	TXD

PC Board Layout Guidelines

The recommended PC board layout for the LPT-11 transceiver and its external components is shown in figure 2.2.

Variations on this suggested PC board layout are possible as long as the general principles of grounding, shielding, guarding, and spacing are employed. For example, using a suitable fixture, the LPT-11 transceiver pins can be formed into a right angle before the transceiver is soldered onto the PC board. In this case, the layout in figure 2.2 would be modified to accommodate horizontal (90°) mounting of the transceiver. If the transceiver is bent to the left in figure 2.2, then C1 should be moved up and to the right, above L1. L1 and C2 can shift down slightly to minimize the trace lengths for L1, C1 and C2 in this variation on the original layout. Note that the ground plane on the solder side of the board becomes more important in this variation since the ground pin of C1 is now on the right-hand side of the transceiver, and a low-impedance path between the ground pins for C1 and C2 is needed.

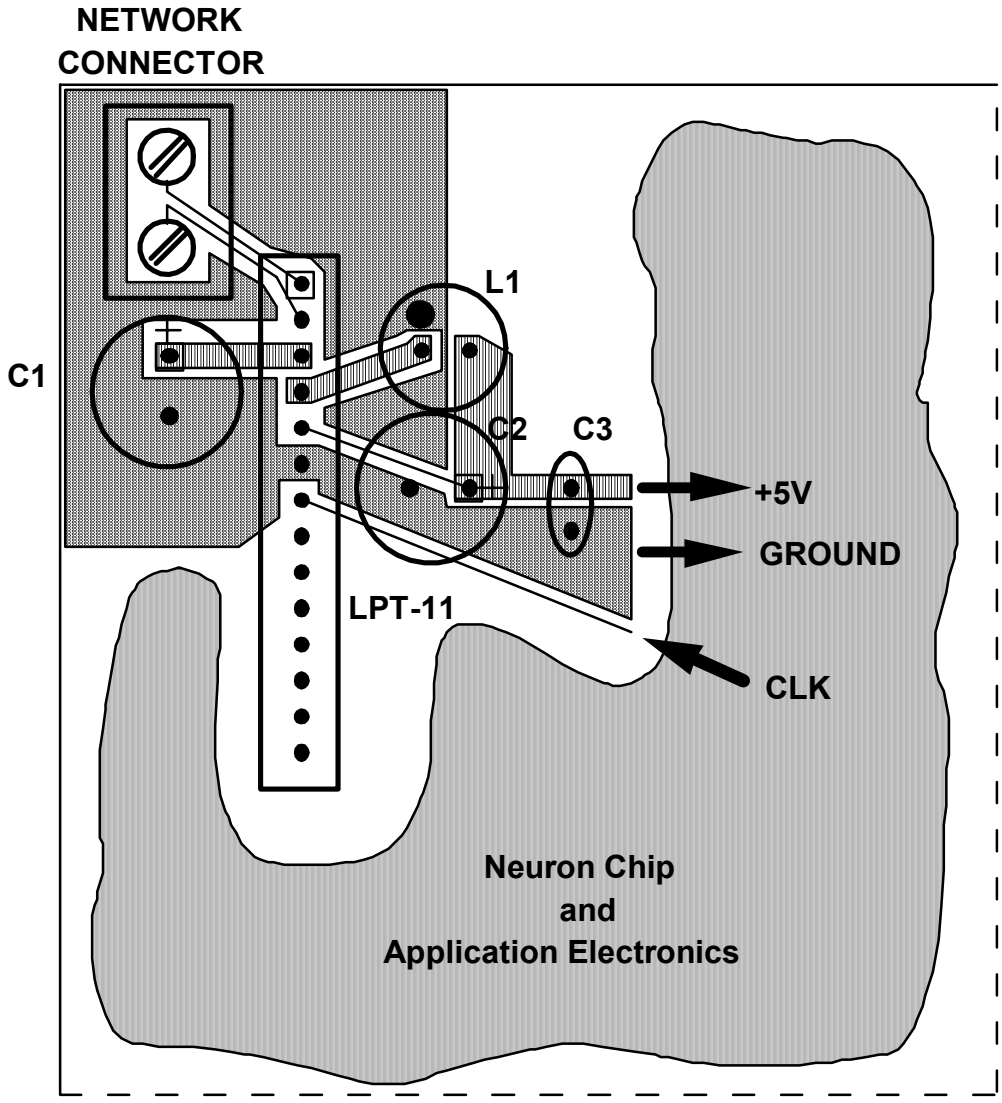

Figure 2.2 Recommended PC Board Layout for LPT-11 Transceiver

Figure 2.2 illustrates the connections between the LPT-11 transceiver and its four power supply-related components on one layer of a two-layer PC board. The other layer (generally the solder side of the board) should contain as much ground plane as possible.

The switching power supply circuit in the LPT-11 transceiver uses the external components L1, C1, and C2 as part of its switching regulator. Because moderate currents are switched at approximately 140kHz, it is very important that L1, C1, and C2 are placed close to the LPT-11 transceiver and oriented as shown in the figure. The inductor L1 and the capacitors C1 and C2 should be placed with minimum gaps to the body of the transceiver. If L1 has exposed ferrite, care should be taken to avoid contact between L1 and the LPT-11 SIP.

The ground connections between the LPT-11 transceiver and L1, C1, and C2 should be as similar as possible to those shown in figure 2.2. The wide ground traces and the ground plane on the other layer of the board serve two functions. First, the wide ground traces reduce inductance to provide a low-impedance path for the power supply switching currents. Second, the wide ground areas minimize electric and magnetic field noise generated by the power supply circuit. The "INDUCTOR" trace from pin 4 of the LPT-11 transceiver to the input of inductor L1 can have voltage signals as high as 35Vp-p at 140kHz. This DC-DC switching waveform may generate moderate levels of electric field noise that can capacitively couple into any nearby high-impedance circuitry. The ground plane is shown close to the "INDUCTOR" trace in order to absorb some of the electric field noise generated by the trace.

Note that L1 is shown in figure 2.2 with a dot marking that is oriented toward the transceiver. In the Taiyo-Yuden LHL08 series of inductors, the dot identifies which pin is connected to the inner portion (beginning) of the cylindrical wire winding on the ferrite slug. Since the input to L1 is a 35V switching waveform and the output is a smooth +5VDC, it is best to orient the inductor so that the windings with the noisy 35V switching waveform are in the inner part of the inductor coil. This uses the inductor coils themselves as part of the electric field shielding. Consult the manufacturer's data sheet for the inductor you are using to determine if polarity marking is available, and whether the marked pin is connected to the inner or outer portion of the coil winding.

If inductor L1 is an "open slug" type without shielding, it often can generate moderate levels of magnetic field noise during normal power supply operation. Ground guarding and a ground plane on the other PC board layer will help to contain the magnetic field noise in a smaller volume near L1. Since the switching frequency of the power supply is near 140kHz, the copper ground plane serves as a fairly effective magnetic field shield.

The electric and magnetic field noise generated by any switching power supply circuit may interfere with the operation of sensitive circuitry nearby. The magnetic field noise can be minimized by using a toroidal inductor for L1, or by using a slug inductor with an integral magnetic shield. Sensitive circuits on a link power device should be laid out to minimize the loop area of any amplifier inputs or high-impedance lines. Minimizing these loop areas reduces the amount of voltage that can be induced in the circuits from the magnetic switching noise that is present. Note that the traces from the network connector to the LPT-11 transceiver as shown

in figure 2.2 are spaced as closely together as possible in order to minimize their loop area. Circuits that are sensitive to electric field noise should be kept away from L1 and pin 4 of the transceiver, and ground guarding should be employed to shield them from the electric field noise.

The +5VDC Vcc trace and GROUND trace are shown leading away from the transceiver into the general board area for the Neuron Chip and application circuit. The Vcc and GROUND should be routed directly off the C2 capacitor to the device's circuitry, as shown. The ground guarding around the network connector should not be used as a source of ground for the digital circuitry. C3 is a small 0.1µF decoupling capacitor that should be placed near C2 to minimize switching noise.

The CLK input to the LPT-11 transceiver (pin 7) needs to be guarded by ground traces to minimize clock noise, and to help keep EMI levels low (see Chapter 6). In general, the Neuron 3120 or 3150 Chip should be placed close enough to the LPT-11 transceiver and oriented correctly so that the CLK trace from the Neuron Chip to the transceiver is no longer than 2cm. At the same time, the Neuron Chip and any other fast digital circuitry should be kept away from the network connector and NET_A/NET_B pins (pins 1 and 2) on the transceiver. If noisy digital circuitry is located too close to the network connector or wires, RF noise may couple onto the network cable and cause EMI problems. With these constraints in mind, it is apparent that the best place to locate the Neuron Chip is in the lower right corner of figure 2.2, with an orientation that places the Neuron Chip's CLK2 line closest to the transceiver's CLK input pin. This position and orientation work well for both the Neuron 3120 and 3150 Chips, since the CP lines are oriented near the lower portion of the LPT-11 transceiver for the rest of the interconnections.

Choosing the Inductor and Capacitors for the LPT-11 Switching Power Supply

Parts that are chosen for L1, C1, and C2 must meet several key specifications to ensure that the switching power supply conversion performed by the LPT-11 transceiver stays within specified limits. As long as these key specifications are met, the designer of a link power device is free to choose parts that have other specifications that best match the application. These specifications allow up to 100mA of sustained peak current to be drawn by the application, including the Neuron Chip. Component selection for low-current applications is discussed in the next section.

Suitable parts for inductor L1 are listed in table 2.3. L1 has the following key specifications that must be met over the device's operating temperature range: L = 1mH ±10%, DCR ≤4Ω, I_{sat} ≥200mA, $F_{res} \geq$ 800KHz. I_{sat} is defined as the DC current at which the measured inductance has not fallen below 80% of its low frequency value, e.g., 800µHenries at 800kHz.

Table 2.3 Examples of L1 Inductor Selections for Consideration (1mH)

Manufacturer (Series)	*Part Number*	*Temperature Range*
Taiyo-Yuden (LHL08)	LHL08-102J	-40°C to +85°C *
TDK (TSL)	TSL0808-102KR26	-40°C to +85°C

The inductors in table 2.3 are unshielded. For compact designs where the components are located very close to one another, Echelon recommends using a shielded construction for L1, in order to minimize the magnetic field interference on nearby transformers, e.g., the FTT-10A transceiver. Contact your inductor manufacturer for availability.

Suitable parts for the V+ input capacitor C1 are listed in table 2.4. C1 has the following specifications that must be met over the device's operating temperature range: C = 100µF ±20%, DCWV ≥63V, I_{ripple} ≥100mA_{rms} @ 100kHz. Echelon recommends the use of a high temperature rated capacitor (105°C minimum) due to the increased component operating life available with this type of construction. The application should determine the need for the extra expense.

Table 2.4 Examples of C1 Capacitor Selections (100µF, ≥63V) For Consideration

Manufacturer (Series)	*Part Number*	*Temperature Range*
Panasonic	EEUFC1J101	-40°C to +85°C
Vishay	EKE00DC310J00	-40°C to +85°C

Manufacturers for the Vcc output capacitor C2 are listed in table 2.5. C2 has the following key specifications that must be met over the device's operating temperature range: C = 22µF ±20%, DCWV ≥ 10V DC Minimum, I_{ripple} ≥ 200mA_{rms} @ 100kHz, ESR (equivalent series resistance) ≤ 1.2Ω Maximum @ 100kHz. Echelon recommends the use of a high temperature rated capacitor (105°C minimum) due to the increased component operating life available with this type of construction. The application should determine the need for the extra expense. Note that the DCWV of capacitors that can meet the ESR requirement are typically rated at greater than 50 VDC. C3 is a small 0.1µF decoupling capacitor that should be placed near C2 to minimize switching noise.

Table 2.5 Examples of C2 Capacitor Selections (22µF, ≥10V, Low ESR) for Consideration

Manufacturer (Series)	*Part Number*	*Temperature Range*
Vishay	EKE00AA222H00	-40°C to +85°C
Nichicon (PL)	UPW1A220MHD	-40°C to +85°C

Alternative Inductor and Capacitor Selection for Low-Current Applications

For applications which require no more than 25mA DC of sustained current, such as a single physical layer repeater using an LPT-11 back-to-back with an FTT-10A, smaller, less-costly surface mount components for L1, C1, and C2 may be substituted for those components noted above. These components should have ratings of -40°C to +85° C minimum. For the C1 and C2 components, Echelon recommends the use of a high temperature rated capacitor (105°C minimum) due to the increased component operating life available with this type of construction.

Table 2.6 Optional Component Selection for Low-Current Applications (up to 25mA)

Component	***Description***
L1	1.0mH, 50mA, 25Ω
C1	22µF, 50V tantalum, 25 mA
C2	22µF, 10V tantalum

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Mechanical Considerations

This chapter discusses the mechanical footprint and connectors of the LPT-11 Link Power Transceiver. Details of mounting the transceiver to an application electronics board containing a Neuron Chip are provided.

Mechanical Footprint

The LPT-11 transceiver mechanical dimensions are shown in figure 3.1. The LPT-11 transceiver is generally mounted to the application board as a through-hole, soldered component. Decisions about component placement on the application electronics board must also consider electromagnetic interference (EMI) and electrostatic discharge (ESD) issues as discussed in Chapter 6 of this document.

Figure 3.1 shows the maximum height of the LPT-11 transceiver as it is shipped from the factory. The user has the option of constructing a fixture to bend the connector pins to reduce the overall height of the printed circuit board assembly on which the transceiver is mounted.

The LPT-11 has a notch on the top edge above Pin 1, as shown in figure 3.1. The fourteen connector pins are fabricated of solder tinned steel alloy.

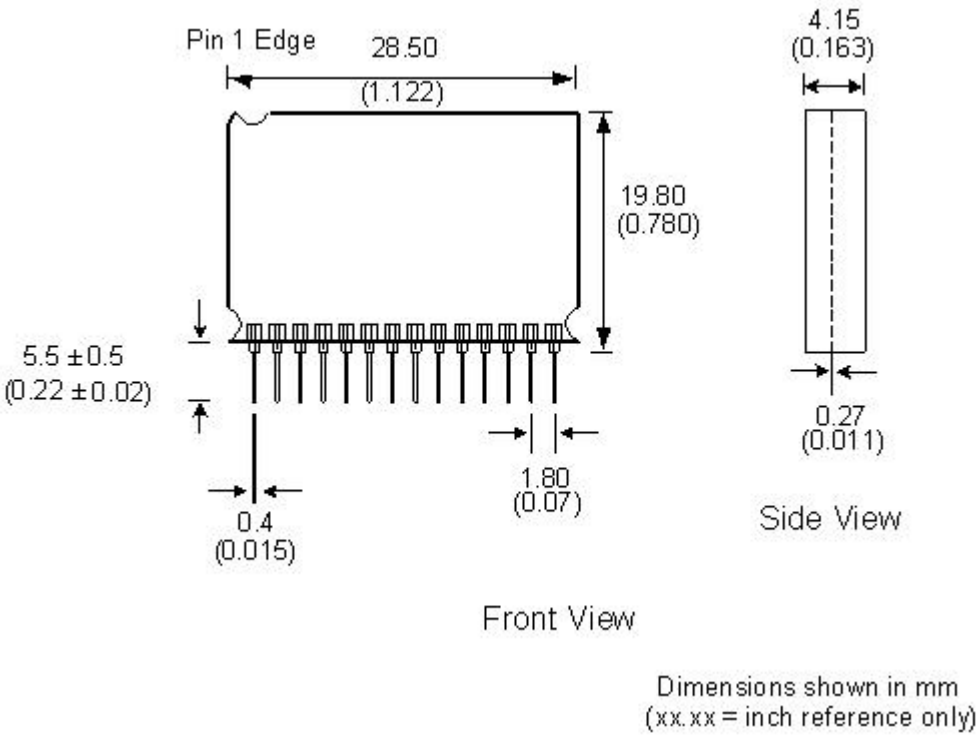

Figure 3.1 LPT-11 Transceiver Mechanical Footprint

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Power Output

This section describes the power supply portion of the LPT-11 Link Power Transceiver, and provides suggestions for using the 5V output current.

Transceiver Output Power

The LPT-11 transceiver power supply circuit performs a number of key functions:

- draws DC power from the twisted pair network without interfering with communications with other devices;
- regulates the output voltage (Vcc) to +5VDC ±5% with a maximum steady state current of 100mA;
- limits Vcc output current to prevent a device with a Vcc short circuit from reducing the network voltage;
- uses an undervoltage shutdown circuit to prevent the transceiver from attempting to start up when the network voltage is too low.

The upper limit of the twisted pair network voltage is 42.4VDC at the output of the LPI-10 module. The actual voltage at the input to the LPT-11 transceiver will be a function of the network wiring topology and the power loading on the network. The LPT-11 transceiver has a lower input voltage limit of ≈26VDC, and the power supply includes an undervoltage detection circuit that will prevent the transceiver from operating at a lower network voltage.

The maximum (sustained peak) output current for the LPT-11 transceiver is 100mA over the full operating temperature range. For applications that come close to this 100mA limit, it is important to measure peak instantaneous current with a current probe (like the Tektronix AM503) rather than with a Digital MultiMeter (DMM). DMMs measure the average current, but they generally cannot follow the rapid current variations associated with digital circuitry. The LPT-11 transceiver's power supply circuit will begin to limit current on any peak instantaneous currents that exceed 100mA, and this will cause a droop in Vcc. Note that the internal circuitry of the transceiver itself derives a small amount of current from the switching power supply directly, and this current consumption does not reduce the 100 mA available current limit.

The power supply is designed to operate without damage in the event of a short between the +5VDC output and GND. Since the LPT-11 transceiver uses a switching power supply to regulate Vcc, the filtering and decoupling requirements of the other powered devices in the device must be considered. A power supply output filter may be required to prevent noise generated by the transceiver's switching power supply from interfering with the operation of these other devices.

As with all switching power supplies, "resonant" current loads on Vcc should be avoided. A resonant load is one that presents large variations in current loading at a continuous repetition rate that is near the switching power supply's switching frequency (or its immediate harmonics or sub-harmonics). An example is a circuit that includes an IR transmitter. The IR LED in a transmitter is typically driven by current pulses ≥ 50mA in amplitude, and with a carrier frequency of 39kHz or 42kHz. These frequencies are close to 1/4 of the LPT-11 transceiver's switching frequency (about 140kHz), so the IR LED driver's power supply may need to be isolated from Vcc with an L-C filter. Typical R-C and L-C filters for isolating loads are shown in figure 4.1

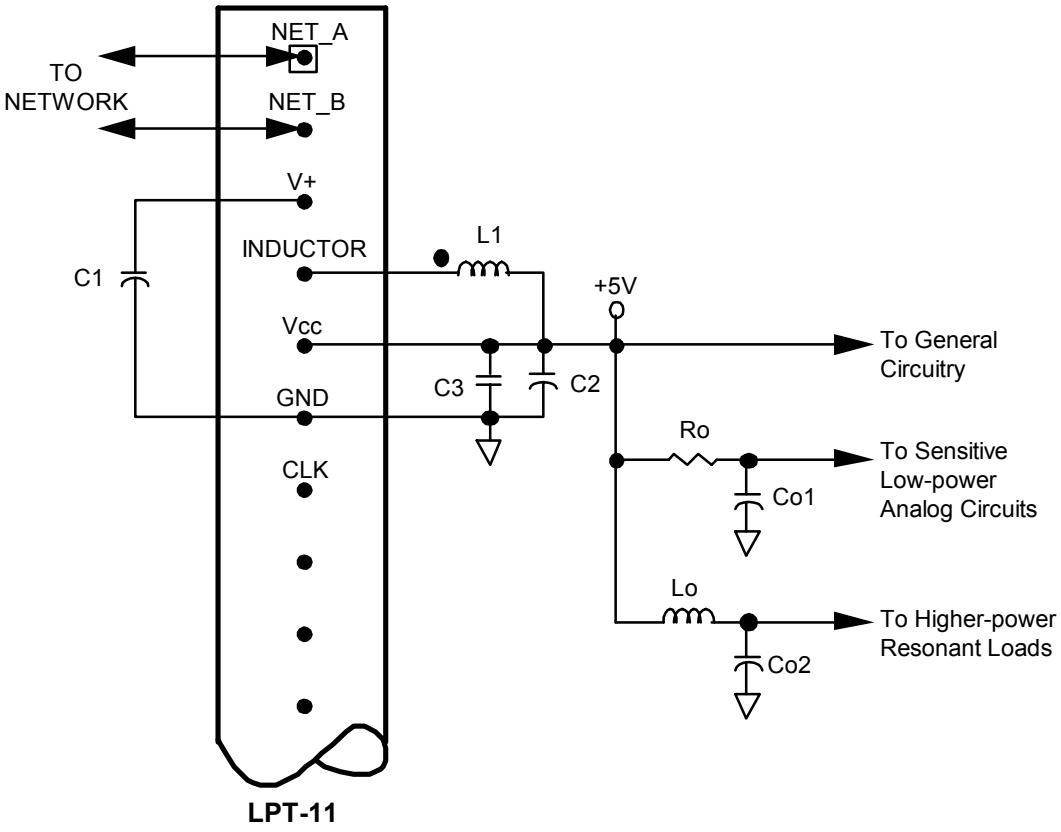


Figure 4.1 Post-Filtering of Vcc

Use the following guidelines to design the resistor and capacitor values for the R-C filter:

1. Set the resistance value R_o as high as possible without causing an excessive voltage drop in the Vcc supplied to the filtered load;
2. Choose the capacitor value C_{o1} to set the cutoff frequency of the R-C filter at least 10x below the frequency (f_n) of noise sensitivity in the circuit being powered. That is, choose $\mathbf{C_{o1} \geq 10/(2\pi R f_n)}$;
3. R_o must be large enough to keep the "effective capacitance" of C_{o1} as seen by the LPT-11 transceiver to less than 5% of the transceiver's 22µF output capacitor C_2. This can be accomplished by ensuring that $\mathbf{R_o \geq 100\Omega(C_{o1}/1\mu F)}$.

The L-C filter should be used for higher-power isolation (when the voltage drop through R would be too high for the application circuit to tolerate). Use the following steps to design the inductor and capacitor values for the L-C filter:

1. Choose an LC product that sets the filter cutoff frequency at least a decade below the frequency of the resonant current demand (f_d) in the load. That is, choose $\mathbf{L_o C_{o2} \geq 100/(4\pi^2 f_d^2)}$;
2. L_o must be large enough to keep the "effective capacitance" of C_{o2} as seen by the LPT-11 transceiver to less than 5% of the transceiver's 22µF output capacitor C_2. This can be accomplished by ensuring that $\mathbf{L_o \geq 1mH(C_{o2}/1\mu F)}$;
3. The inductor's series resistance must be small enough so that the load current flowing through it does not generate excessive voltage drop. Choose an inductor value L_o that has a low enough DC resistance (DCR in the manufacturer data sheets) for your load current. Generally, smaller inductors cost less, so you will want to choose the smallest value of L_o that meets the above criteria;
4. Once L_o is set, the value of C_{o2} can be chosen subject to the conditions in steps 1 and 2 above.

Finally, it is good design practice to decouple each IC's Vcc pin in the device circuit using 0.1µF or 0.01µF radial or surface mount capacitors. This decoupling helps to reduce Vcc noise that could lead to logic noise problems and radiated EMI problems (see Chapter 6 for more information on design hints to reduce EMI).

WARNING: THE COMBINED CAPACITANCE OF ALL THE DECOUPLING CAPACITORS (FROM VCC TO GND) SHOULD NOT EXCEED 1.0µF. TOTAL DECOUPLING CAPACITANCE IN EXCESS OF 1.0µF CAN CAUSE UNSTABLE POWER SUPPLY PERFORMANCE.

Powering Non-Isolated Devices

In order to provide reliable common mode rejection, the link power system operates with one earth ground connection at the LPI-10 module, and all LPT-11 transceivers are isolated (floating) relative to ground. The LPT-11 transceiver power supply is designed to power devices that are ground isolated. If the power supply is connected to a grounded device, both network communications and power distribution will be degraded. For devices where the application electronics must be connected to earth ground, the FT 31xx Smart Transceiver is the best choice, providing both isolation and communication with LPT-11 devices on the same twisted pair network segment. Optionally, optical isolation may be used between the application electronics and Neuron Chip.

Note that only floating measurement instruments should be used when working with link power devices when power is applied. Only isolated Digital Volt Meters (DVMs), floating differential probes (e.g., HP 1141A) or battery-powered oscilloscopes (e.g. THS 720 Series TEKSCOPE) should be used when working with link power devices. The LPT-11 transceiver may be damaged if its circuitry is inadvertently shorted to earth while power is applied.

5

Network Cabling and System Performance

This chapter provides information about cabling and network connections for the LPT-11 Link Power Transceiver. This information includes a discussion of wire characteristics and power distribution issues.

Network Overview

The link power system is designed to support free topology wiring, and will accommodate bus, star, loop, or any combination of these topologies. LPT-11 transceivers can be located at any point along the network wiring, as can the LPI-10 module and its associated power supply. This capability simplifies system installation and makes it easy to add devices should the system need to be expanded. Figures 5.1 through 5.5 present five different network topologies.

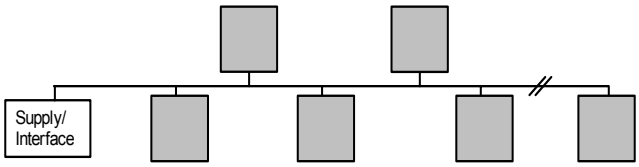


Figure 5.1 Singly Terminated Bus Topology

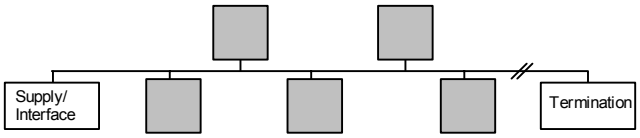


Figure 5.2 Doubly Terminated Bus Topology

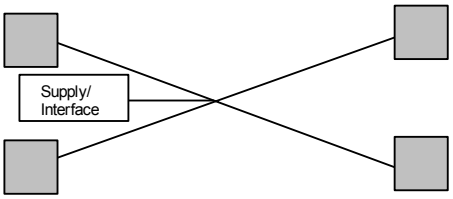


Figure 5.3 Star Topology

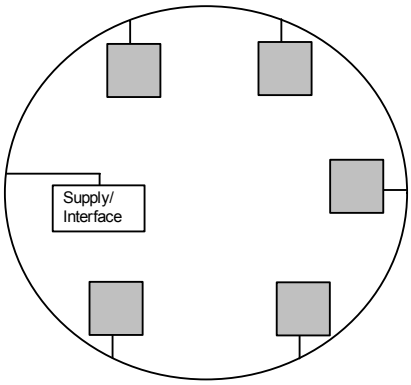


Figure 5.4 Loop Topology

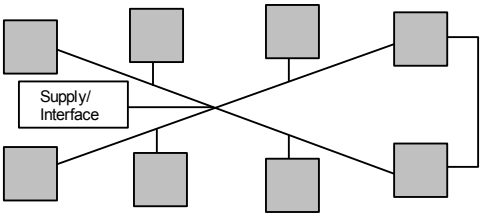


Figure 5.5 Combination Loop/Bus Topology

In the event that the limits on the number of transceivers or total wire distance are exceeded, then a link power physical layer repeater can be added to interconnect two link power systems and double the overall system capability (see Appendix A). Echelon's media routers can also be used to interconnect the link power system with any other LONWORKS channel.

System Performance and Cable Selection

Link power performance has system, transmission, and power specifications which are outlined on the following pages. Each of the specifications should be met to ensure proper operation.

The system designer may choose a variety of cables, depending on cost, availability and performance. Performance as outlined in the transmission and power specifications varies with cable type. The wire resistance per unit length is a significant factor in the power specification, since the system is designed to accommodate a substantial drop in voltage along the wire according to Ohm's Law. The transmission specification depends on such factors as resistance, mutual capacitance, and the velocity of signal propagation.

Echelon has characterized system performance on several cable types whose typical electrical parameters are shown in table 5.1.

Table 5.1 Cable Parameters

Cable Type	Wire dia. /AWG	R_{loop} Ω/km	C nF/km	Vprop % of c
Belden 85102, single twisted pair, stranded 9/29, unshielded, plenum	1.3mm/16	28	56	62
Belden 8471, single twisted pair, stranded 9/29, unshielded, nonplenum	1.3mm/16	28	72	55
Level 4/22AWG, twisted pair, typically solid & unshielded	0.65mm/22	106	49	67
JY (St) Y 2x2x0.8, 4-wire helical twist, solid, shielded	0.8 mm/20.4	73	98	41
Category 5, UTP, EIA/TIA 568A	0.5mm/24	168	50	58

If the cable has a shield, it should be connected to the LPI-10 module ground (at the P1 connector) via a 470kΩ, 1/4 Watt, ≤ 10%, metal film resistor to prevent static charge build-up.

For more information on Level 4 cable, go to the Underwriters Laboratories Inc. website at www.ul.com.

Note that the specifications in Transmission Specifications *are for one network segment. Multiple segments may be combined using repeaters as described in Appendix A to increase the number of devices, application current, and distance. For example, a free topology network containing 256 link power devices and total wire length of up to 500 meters may be built using two segments interconnected by a repeater, assuming network traffic requirements are met. See limitations in Appendix A.*

System Specifications

- Up to 128 LPT-11 transceivers or 64 FTT-10A/FT 31xx transceivers are allowed per network segment.
- 1 Link Power Unit Load (LPUL) = 25ma@Vcc=5V. Therefore, 4 LPULs = 100ma, the recommended maximum for a single LPT-11 transceiver.
- Both types of transceivers may be used on a given segment, provided that the following constraint is met:
  (1 x number of LPT-11 transceivers) + (2 x number of FTT-10A transceivers) ≤ 128
- The average temperature of the wire must not exceed +55°C, although individual segments of wire may be as hot as +85°C.
- The sum of the application current of all the devices in a segment must not exceed 3.2A at +5V.

Transmission Specifications

Table 5.2 Doubly-Terminated Bus Topology Specifications

	Maximum bus length	***Maximum stub length***	***Units***
Belden 85102	2200	3	meters
Belden 8471	2200	3	
Level 4/22AWG	1150	3	
JY (St) Y 2x2x0.8	750	3	
Category 5	725	3	

Table 5.3 Free Topology Specifications

	Maximum total wire length per network segment	***Units***
Belden 85102	500	meters
Belden 8471	400	
Level 4/22AWG	400	
JY (St) Y 2x2x0.8	320	
Category 5	400	

The *maximum total wire length* is the total amount of wire connected per network segment. This means the sum of all wire lengths used, not simply the wire in the path between two devices. The maximum *device-to-device* distance is only limited by the maximum total wire length.

Power Specifications, Simplified Form

A link power network allows for multiple branches, e.g., a star topology. A *branch* is defined as any length of twisted pair cable that extends from the LPI-10 module. Loop topologies can be formed by joining the ends of branches.

Whereas system and transmission distance specifications involve the entire network, power specifications apply to individual branches. The closer the devices on a branch are to the LPI-10 module, the more devices that can be on that branch. Similarly, the fewer the devices on a branch, the longer that branch can be.

Both nominal and worst case power specifications for the performance of the link power system, with both lumped and distributed loads, are shown in tables 5.4 through 5.7.

The following section, "Power Specifications for Extended Performance," may be used as an alternative to tables 5.4 through 5.7. It is more complex, but will allow better performance for certain topologies.

Multiple link power segments may be interconnected via physical layer repeaters or LONWORKS routers to extend distance, number of devices, and total available application current.

Table 5.4 Simplified Power Specifications Using Belden 85102 or Belden 8471 (16AWG/1.3mm) Wire

		Nominal	*Worst Case*	*Units*
500 meter branch length, Evenly distributed loading along a bus				
application current:	25 mA	128	128	devices
	50 mA	64	64	
	100 mA	32	32	
500 meter branch length, Lumped loading or otherwise distributed				
application current:	25 mA	112	81	devices
	50 mA	56	40	
	100 mA	28	20	
400 meter branch length, Lumped loading or otherwise distributed				
application current:	25 mA	128	101	devices
	50 mA	64	50	
	100 mA	32	25	

Table 5.5 Simplified Power Specifications Using JY (St) Y 2x2x0.8 Wire

		Nominal	*Worst Case*	*Units*
320 meter branch length, Evenly distributed loading along a bus				
application current:	25 mA	128	96	devices
	50 mA	64	48	
	100 mA	32	24	
320 meter branch length, Lumped loading or otherwise distributed				
application current:	25 mA	64	48	devices
	50 mA	32	24	
	100 mA	16	12	
160 meter branch length, Lumped loading or otherwise distributed				
application current:	25 mA	128	96	devices
	50 mA	64	48	
	100 mA	32	24	

Table 5.6 Simplified Power Specifications Using Level 4/22AWG (0.65mm) Wire

		Nominal	***Worst Case***	***Units***
400 meter branch length, Evenly distributed loading along a bus				
application current:	25 mA	74	53	devices
	50 mA	37	26	
	100 mA	18	13	
400 meter branch length, Lumped loading or otherwise distributed				
application current:	25 mA	37	26	devices
	50 mA	18	13	
	100 mA	9	6	

Table 5.7 Simplified Power Specifications Using Category 5 Wire

		Nominal	***Worst Case***	***Units***
400 meter branch length, Evenly distributed loading along a bus				
application current:	25 mA	47	34	devices
	50 mA	23	17	
	100 mA	12	8	
400 meter branch length, Lumped loading or otherwise distributed				
application current:	25 mA	23	16	devices
	50 mA	11	8	
	100 mA	6	4	

Power Specifications for Extended Performance

Although more complex, this alternative power specification allows for extended power performance. In addition, it features a separate derating for the average wire temperature.

I is the average application current of a device. The distance of an LPT-11 transceiver from the LPI-10 module is the **device distance**, **d**. For each branch, the sum of the products of a device distance and the application current of that device must not exceed a constant:

$$I_1 * d_1 + I_2 * d_2 + I_3 * d_3 + \ldots \leq K * \alpha$$

where

K is the nominal value, dependent on wire type:

K=1135 Amp*Meters for Belden 85102 and Belden 8471, 16 AWG

K=430 Amp*Meters for JY (St) Y 2x2x0.8

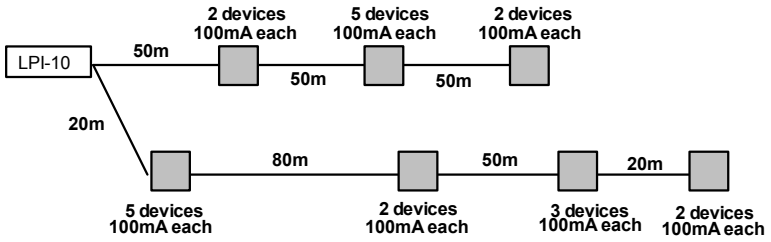
K=300 Amp*Meters for Level 4/ 22AWG

K=190 Amp*Meters for Category 5

$$\alpha = \frac{1}{1 + 0.00393 * (temp - 25°C)}$$ **, accounting for average wire temperature**

At 25°C, $\alpha = 1$. Note that α is greater than one when average wire temperature is less than 25°C and is less than one when the temperature is greater than 25°C.

In the following example, there are only two branches to check. Assume wire type is JY (St) Y 2x2x0.8 and average wire temperature is 25°C. Thus, $\alpha = 1$.



In the upper branch,

$$(2*0.1A)(50m) + (5*0.1A)(100m) + (2*0.1A)(150m)$$
$$= 90 \text{ Amp*meters}$$
$$\leq K*\alpha = (430 \text{ Amp*meters})(1) = 430 \text{ Amp*meters}$$

In the lower branch,

$$(5*0.1A)(20m) + (2*0.1A)(100m) + (3*0.1A)(150m) + (2*0.1A)(170m)$$
$$= 109 \text{ Amp*meters}$$
$$\leq K*\alpha = (430 \text{ Amp*meters})(1) = 430 \text{ Amp*meters}$$

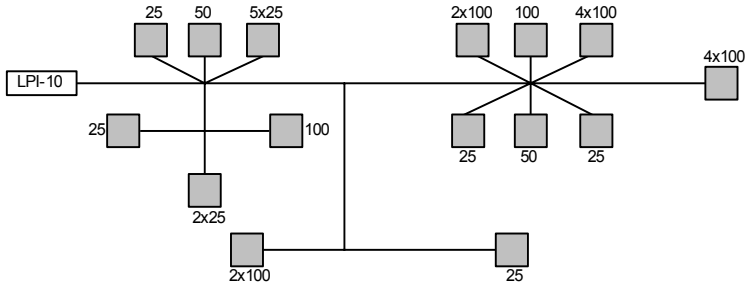
This network meets all system, transmission, and power specifications.

In many instances, the lengths of sub-branches can be ignored for this calculation, reducing the effective **d** and improving performance.

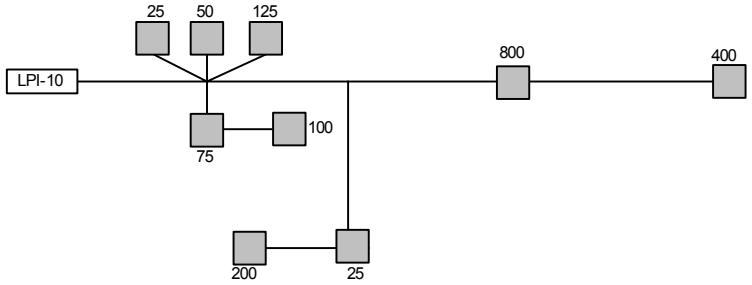
To determine when the lengths of stubs or sub-branches can be ignored for power calculation, begin at the ends of the branches and move toward the LPI-10 module. Upon arriving at a branching point, calculate the sum of products $(I_1*d_{s1} + I_2*d_{s2} + \ldots)$ for every sub-branch where **I** is the application current of a device and d_s is the distance of that device from the branching point. Then ignore the lengths of all the sub-branches except for the sub-branch with the largest sum of products. Repeat this procedure until the effective network looks like a bus (see Step Three of Example 1, on the following page). Note that this simplification may be used only for power considerations. For transmission specifications, the actual total wire length and maximum distance device-to-device must be used.

Example network 1, below, illustrates the simplification process in three steps. Distances are drawn in relative proportion. The numbers represent +5V application currents, with 5x25 indicating 5 devices of 25mA each at the same location. Use the equivalent power network from Step Three when applying the extended power performance specification.

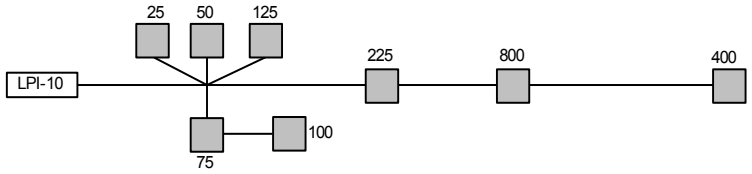
Example 1. Actual Network:



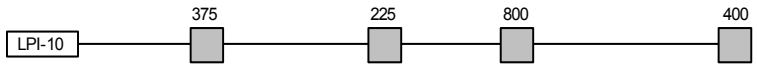
Simplification Step One:



Simplification Step Two:



Simplification Step Three and equivalent network for power specifications:

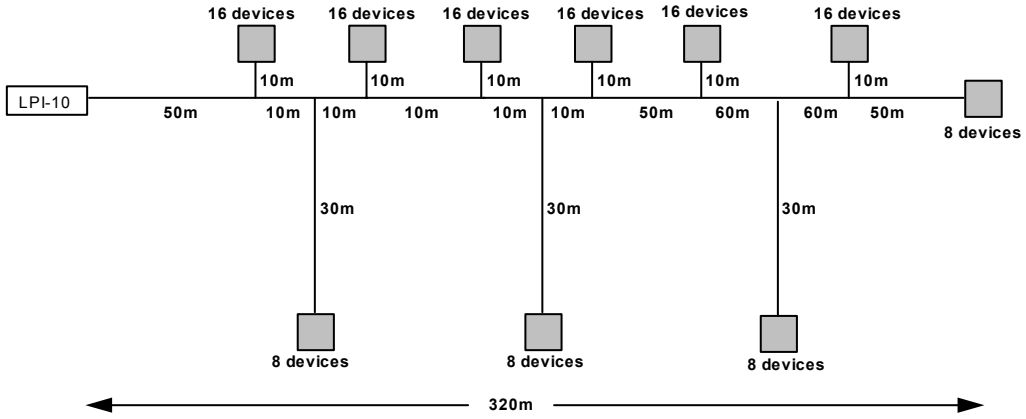


Here is a second example that illustrates the benefits of the extended performance specification and the importance of the sub-branching simplification procedure. Without simplifying the network, the sample topology fails to meet the power specification. However, the equivalent power network, which ignores the lengths of all but one of the sub-branches, meets the worst case extended performance power specification and is therefore an allowable topology.

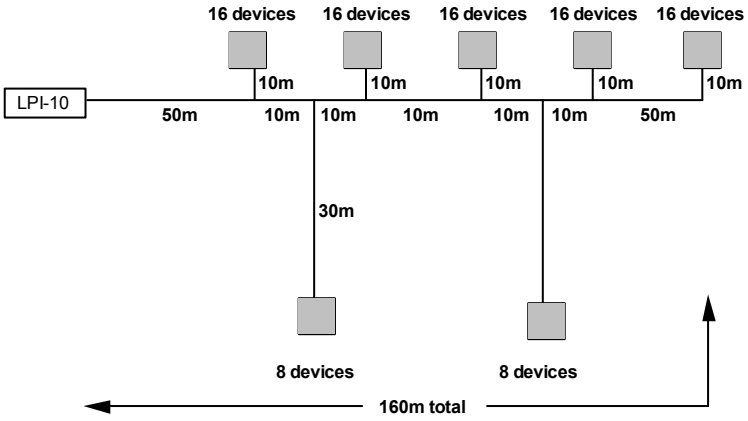
If the simplified form of the power specification is used instead, the actual network below would not be allowed. Table 5.4 (worst case) allows only a truncated version of the network, which has 96 devices and a 160 meter branch length, instead of 128 devices and a 240 meter branch length.

All devices have 25 mA (1 LPUL) of application current. The wire type is JY (St) Y 2x2x0.8 and average wire temperature is 25°C.

Example 2. Actual Network, allowed by extended performance power specification:



Truncated network, allowed by table 5.4 (worst case):



Cable Termination

A link power network segment requires termination for proper data transmission performance. A total termination impedance of approximately 52Ω is required.

Free Topology Segment

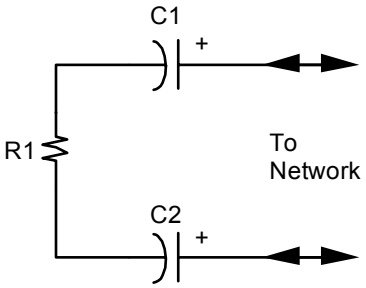
In a free topology segment, only one termination is required and may be placed anywhere on the free topology segment. The LPI-10 Link Power Interface, with jumper at "1 CPLR" setting, provides this termination.

Doubly Terminated Bus Topology Segment

In a doubly terminated bus topology, two terminations are required, one at each end of the bus.

1. The LPI-10 Link Power Interface, with jumper at "2 CPLR" setting, provides one termination.

2. An RC network (figure 5.6) provides the second termination.



C1, C2	100µF, ≥50V
R1	105Ω, 1%, 1/8W

Note: Observe polarity shown for C1 and C2.

Figure 5.6 RC Network

Commissioning LPT-11 Transceivers

LPT-11 transceivers can be connected to any point of the twisted pair cable provided that the total wire and power limits are not exceeded. This design makes it simple to install both new systems and to expand existing systems. The LPT-11 transceiver is an electronic component and the installer should exercise reasonable care when commissioning any electronic device. For more information on commissioning a link power system and procedures for network fault isolation, consult the *LONWORKS LPI-10 Link Power Interface Module User's Guide*.

6

Design Issues

This chapter looks at design issues, and includes discussions of Electromagnetic Interference (EMI), Electrostatic Discharge (ESD), and surge for the LPT-11 Link Power Transceiver.

EMI Design Issues

The high-speed digital signals associated with microcontroller designs can generate unintentional Electromagnetic Interference (EMI). High-speed voltage transitions generate RF currents that can cause radiation from a product if a length of wire or piece of metal can serve as an antenna.

Products that use the LPT-11 transceivers together with a Neuron Chip will generally need to demonstrate compliance with EMI limits established by various regulatory agencies. In the USA, the FCC requires that unintentional radiators comply with Part 15 level "A" for industrial products, and level "B" for products that can be used in residential environments. Similar regulations are imposed in most countries throughout the world.

Designing Systems for EMC (Electromagnetic Compatibility)

Careful design of application electronics is important to ensure that an LPT-11 transceiver will achieve the desired level of EMC. In a link power network, the devices "float" relative to local safety/earth ground because the single point of earth ground in the network is at the LPI-10 module. Since no explicit connection to earth ground is allowed at a link power device, the usual EMC techniques involving grounding do not apply. The techniques for designing RF-quiet link power devices are very similar to those used with battery-powered palmtop computers, since palmtops have no explicit earth ground connection and have cables that connect them to other devices.

Since link power devices are not allowed to have an explicit earth ground connection, it becomes very important to minimize the "leakage" capacitance from circuit traces in the device to any external pieces of metal near the device. Figure 6.1 shows the leakage capacitances to earth ground from a device's logic ground ($C_{leak,GND}$) and from a digital signal line in the device ($C_{leak,SIGNAL}$).

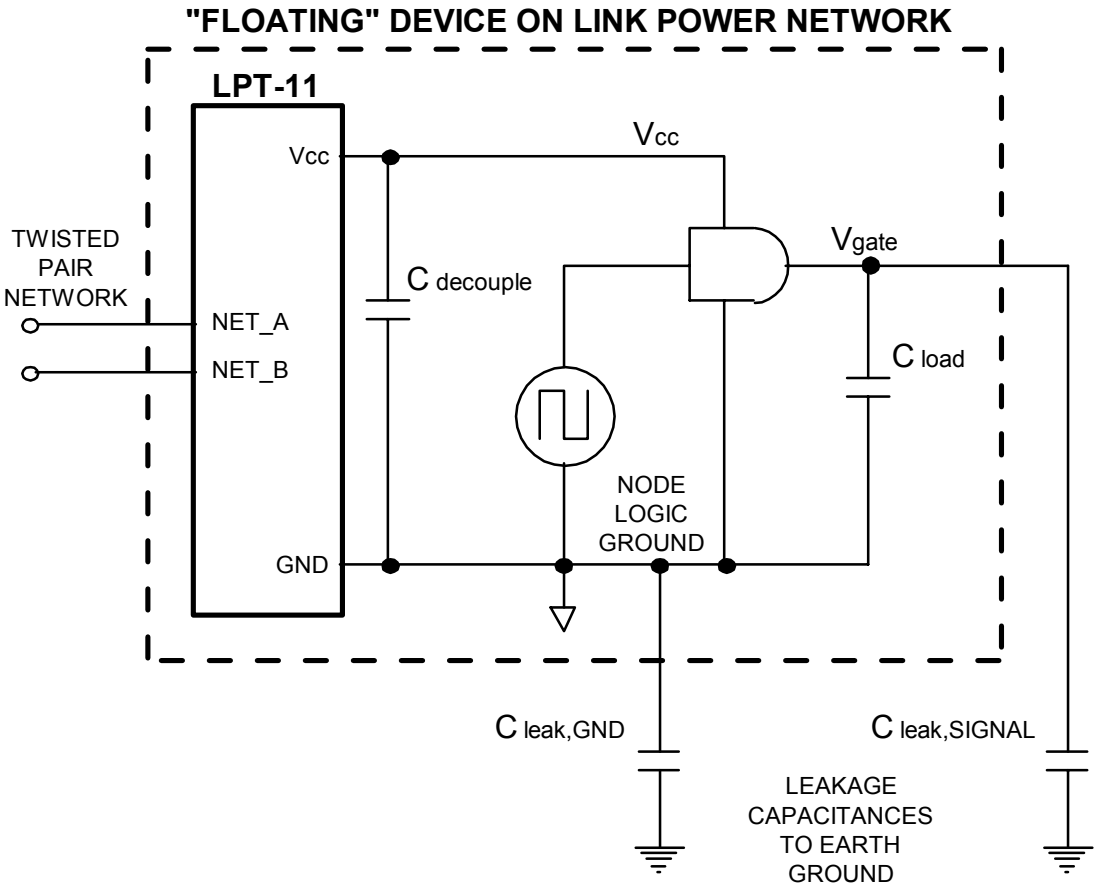


Figure 6.1 Parasitic Leakage Capacitances to Earth Ground

The single most important technique for designing an EMI "quiet" floating device is to use logic ground to guard any fast digital signal lines. Effective guarding of traces with logic ground reduces $C_{leak,SIGNAL}$ significantly, which in turn reduces the level of common-mode RF currents driven onto the network cable.

When a device is mounted near a piece of metal, especially metal that is earth grounded, any leakage capacitance from fast signal lines to that external metal will provide a path for RF currents to flow. When V_{gate} is pulled down to logic ground, the voltage of logic ground with respect to earth ground will increase slightly. When V_{gate} pulls up to Vcc, logic ground will be pushed down slightly with respect to earth ground. As $C_{leak,SIGNAL}$ increases, a larger current flows during V_{gate} transitions, and more common-mode RF current couples to the network twisted pair. This common-mode RF current can generate EMI in the 30-300MHz frequency band in excess of "B" levels even when $C_{leak,SIGNAL}$ from a clock line to earth ground is less than 1pF, so guarding of clock lines is essential for meeting Level "B" requirements.

From this discussion, it is apparent that minimizing $C_{leak,SIGNAL}$ is very important. By using 0.1µF or 0.01µF decoupling capacitors at each digital IC power pin, Vcc and logic ground noise can be reduced. Logic ground can then be used as a ground shield for other noisy digital signals and clock lines.

For example, in most link power devices that use the Neuron 3120 Chip, the only fast digital signal that needs to be routed across the PC board is the CLK2 line from the Neuron Chip to the LPT-11 transceiver (CLK on transceiver pin 7, see figure 2.1). If a two-layer PC board is being used, CLK2 can be routed to the transceiver pin with ground guard traces straddling the clock trace on the component side of the board, and a wide ground trace (or ground plane) covering the underside of the clock trace on the solder side of the PC board. If a four-layer PC board is being used, the clock trace can be buried in an inner layer and guarded on all four sides. The CLK2 trace from the Neuron Chip to the LPT-11 transceiver should be as short as practical, and in all cases ≤ 2cm. Pin 8 of LPT-11, a no-connect pin, can also be connected to GND to provide shielding up to the LPT-11 module.

It may be possible to minimize $C_{leak,SIGNAL}$ by spacing the device's circuitry away from any nearby metal using a plastic package or standoffs, and there may be some mechanical configurations where there will never be earth ground near a link power device, i.e., motion sensors that hang from ceilings. For most devices, though, logic ground guarding of fast digital signals will be required to meet "B" levels of EMC.

Since the Neuron 3150 Chip has an external memory interface bus, there are many more traces in a Neuron 3150 Chip-based link power device that need to be guarded by logic ground. In addition, the Vcc noise generated by the memory interface and external ROM/RAM components requires more Vcc decoupling, and may require a four-layer PC board to maintain an RF-quiet Vcc and logic ground.

If the link power device's application circuitry uses fast digital signals, the same EMC design rules apply. Some link power devices with fast circuitry such as DSP engines and memory arrays, etc. may require extra RF attenuation between the LPT-11 transceiver and the twisted pair network in order to meet level "A" or "B". This extra attenuation can be provided by a common-mode ferrite choke in series with the NET_A and NET_B lines near the network connector. A common-mode ferrite choke, such as muRata's PLT09H-2003R, can provide an additional 10-15dB of attenuation over the 30-300MHz RF band. Note that a common-mode choke must be used because of the differential DC current (≤50mA) that the LPT-11 transceiver draws from the network to power the device. If individual ferrite beads are used on the NET_A and NET_B lines, they must be large enough not to be saturated by this DC network current flowing into the device.

In summary, the following general trends apply for link power EMC:

- the faster the Neuron Chip clock speed (2.5MHz to 20MHz), the higher the level of EMI;
- better Vcc decoupling quiets RF noise at the sources (the digital ICs), which lowers EMI;
- the Neuron 3120 Chip will generate less EMI than the Neuron 3150 Chip since the 3120 has no external memory interface lines;
- a four-layer PC board will generate less EMI than a two-layer PC board since the extra layers facilitate better Vcc decoupling and more effective logic ground guarding;
- a two-layer link power device based on a 5MHz Neuron 3120 Chip should be able to meet FCC/VDE level "B" EMC if good decoupling and ground guarding of the CLK2 line are used;

- a common-mode ferrite choke can be used to help meet EMC requirements for devices that have noisy application circuitry or special circuit requirements.

Note that it may be possible to design a two-layer 10MHz Neuron 3150 Chip-based link power device that will pass level "B" in some applications, depending on the mechanical configuration. Early testing of prototype circuits at an outdoor EMI range should be used to determine the effectiveness of these EMC techniques in a particular application.

ESD Design Issues

Electrostatic Discharge (ESD) is encountered frequently in industrial and commercial use of electronic systems. Reliable system designs must consider the effects of ESD and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. The static voltages generated by humans can exceed 10kV. Keyboards, connectors, and enclosures provide paths for static discharges to reach ESD sensitive components such as the Neuron Chip. This section describes techniques to design ESD immunity into LPT-11 transceiver-based products. For a discussion of ESD issues for the LPI-10 module, see the *LONWORKS LPI-10 Link Power Interface Module User's Guide*, part number 078-0104-01.

ESD testing is important to ensure that a link powered device and its network connection can withstand real-world exposure to static discharges. In addition, the European Community has adopted legal requirements for ESD testing of products.

Designing Systems for ESD Immunity

As with the EMI design issues discussed above, ESD hardening of link power devices is different than hardening products that have an explicit earth ground connection. If $C_{leak,GND}$ can be kept small (say, ≤ 5pF), and if the link power device is housed inside a plastic enclosure that offers no access for ESD hits (as in an enclosed IR motion sensor), then ESD testing is fairly easy to pass. The current from static discharges to the device's network connector will travel out the network cable, with very little energy coupled into the device's circuitry.

In devices that have a larger $C_{leak,GND}$ (up to about 20pF), more energy travels from network connector ESD hits through the LPT-11 transceiver's ESD protection circuitry to logic ground, and from there to earth ground through $C_{leak,GND}$. In this type of device, it is important to lay out the ground plane and ground guarding so that the LPT-11 transceiver's ground (pin 6) is connected directly to the largest section of the ground plane without any sensitive circuitry in the path. When the ESD hit is directed into logic ground by the LPT-11 transceiver, the transient current can flow out to earth ground via $C_{leak,GND}$ without causing disruptive voltage bounces in other device circuitry.

ESD hits should not be allowed to reach a link power device's internal circuitry. Adequate creepage and clearance distances should be built into each device's enclosure to prevent discharges to anything other than the network wiring

connector. If metal must be accessible on the outside of a device's enclosure, then it may be necessary to provide an earth ground connection to that metal. For example, if metal toggle switches must be user-accessible, then it may be necessary to mount the switches on a metal plate that is earth grounded. In this way, ESD hits to the toggle switch handles will be diverted to the local earth ground. The device's logic ground must still remain isolated from this earth-grounded "guard" plate, and the leakage capacitance from logic ground to earth ground ($C_{leak,GND}$) should be held below about 10-20pF to minimize damage from network ESD hits.

Surge Design Issues

Surge voltages encountered in industrial and residential environments as a result of nearby AC mains switching transients and lightning can cause disturbances or failures of electronic communications systems. Transient voltages and currents can couple capacitively or magnetically to the twisted pair wiring of the link power system. Physical construction of twisted pair wire causes transients to couple to the cable in a common-mode fashion, i.e., both conductors of the wire pair see the same transient. Since link power devices float with respect to earth and communication occurs in a balanced (symmetric) fashion, common-mode transients have minimal effect on transmission.

The single point of earth reference for a link power network segment is the LPI-10 module. When the LPI-10 module clamps an incident voltage transient, a residual differential transient voltage may result across the twisted pair conductors. This residual voltage is seen by the LPT-11 devices. For small transient voltages found in benign environments no additional protection for LPT-11 devices is required. However, additional protection is required to prevent higher energy transients from damaging LPT-11 devices. This section describes the recommended protection scheme necessary to achieve immunity for link power devices to various levels of transient voltages defined by the EN61000-4-5 EMC Surge immunity requirements specification.

Designing Systems for Surge Immunity

Adequate creepage and clearance distances must be built into each device's enclosure to prevent surge discharges from the local LPT-11 transceiver logic ground to earth.

LPT-11 transceivers are immune to EN-61000-4-5 surge test level 1 (0.5kV). Level 2 (1.0kV) and level 3 (2.0kV) surge immunity can be attained with the addition of a bi-directional transient voltage suppresser (TVS). The TVS must be placed directly across Net_A and Net_B lines at each LPT-11 (not for use between either of the data lines and earth).

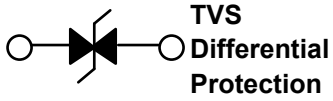


Figure 6.2 TVS Schematic Symbol

TVS devices used with LPT-11 transceivers must meet the following requirements:

- bi-directional protection;
- rated at 400W minimum peak power (10/1000μs waveform) rating;
- working peak reverse voltage rating $V_{rwm} \geq 42.4V$ (-40°C to +85°C); V_{rwm} should be as low as possible over the temperature range but not less than 42.4V. Typical reverse breakdown voltage ratings, V_{br}, for such devices will be approximately 53V;
- bi-directional capacitance $C \leq 275pF$ @Vr = 26V; bi-directional capacitance in this application is typically 80% of data book unidirectional rating. Capacitance increases as voltage across the device decreases.

Table 6.1 lists recommended TVS devices for use with LPT-11 transceivers. Note that bi-directional devices must be used.

Table 6.1 Recommended TVS Devices

Manufacturer	Part Number	Peak Power	Package
Fairchild	SA45(c)A	500W	Axial
Vishay	SA45A	500W	Axial

Building Entrance Protection

Echelon recommends using shielded twisted pair wire for all networks, or portions of networks, that are run outside of buildings. The shield should be connected to earth at each building entry point via a data lightning/surge arrester, to conduct excessive surges or lightning strike energy to ground and prevent their entry inside the building via the network. Data line lightning/surge arresters should also be used at each building entrance and connected to the network data lines. Therefore, two arresters, one for each conductor of the twisted pair, are required, and Echelon recommends the use of the gas discharge type. The gas discharge type of arrester presents extremely low capacitance to the transmission line, minimizing possible corruption of the network data traffic. MOV and TVS protection devices should not be used in this way because their intrinsically high capacitance as well as low matching tolerance will likely create imbalance in the transmission line, preventing network data traffic. However, TVS devices from Table 6.1 may be connected *differentially* across the network for surge protection.

Gas discharge devices are typically used for data line lightning/surge arresters due to their very low capacitance (typically < 5pF) and rapid response. Use of this type of device will not reduce the number of possible nodes used on a network segment. Since there is minimal amount of "leakage capacitance" or unbalance to ground allowed in a link power network, the two arresters used should match (be balanced) within 10pF.

The following figure depicts twisted pair networks running in outdoor locations.

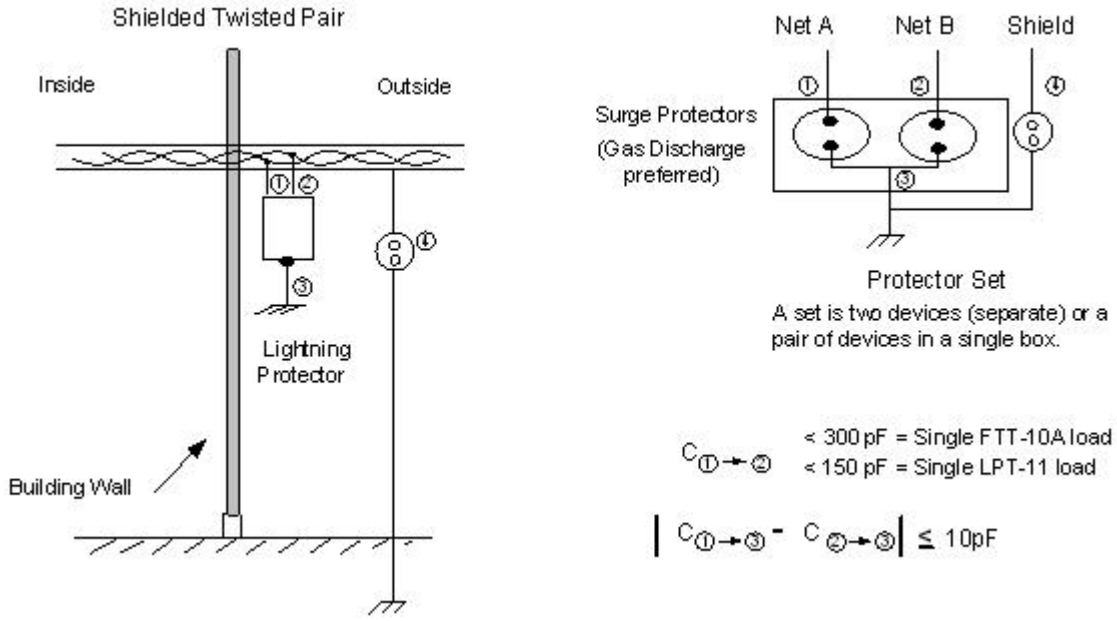


Figure 6.3 Network and Shield Lightning Protection

For maximum surge protection, **every** LPT-11 link power device on the network segment, whether located indoors or outdoors, has the protection circuitry described in the previous section. This is in addition to any building entrance protection devices present on the network.

EN 61000-4 Electromagnetic Compatibility (EMC) Testing

Echelon has tested the LPT-11 transceiver operating in typical two-layer application boards to verify that the transceiver complies with the five applicable EN 61000-4 test requirements (formerly known as IEC 1000-4 tests). Provided that a device's PCB is designed following the guidelines in Chapter 2, the LPT-11 transceiver should pass the EN 61000-4 tests described in table 6.2.

Table 6.2 EN 61000-4 Test Immunity Levels

EN Test	***Description***	***LPT-11 Immunity Level***
EN 61000-4-2	ESD	Level 4
EN 61000-4-3	Radiated Susceptibility	Level 2
EN 61000-4-4	Burst	Level 4
EN 61000-4-5	Surge	Level 3*
EN 61000-4-6	Conducted RF Immunity	Level 3

* Level 3 may be obtained with addition of TVS between NET_A and NET_B.

EN 61000-4-2 ESD testing is performed on a metal test table using an ESD transient generator. Level 4 testing involves injecting up to ±8kV contact discharges and up to ±15kV air discharges into the product under test. Depending on the product design, discharges may be injected at the network connector, power connector and other user-accessible areas. Under the test, proper operation continues with occasional loss of a packet and infrequent device resets.

EN 61000-4-3 RF Susceptibility testing is generally performed in an RF-shielded anechoic chamber. The product under test is placed on a non-conducting table in the chamber, and antennas are used to subject the product to intense radio frequency fields. Under the test, proper operation continues with occasional loss of a packet. Level 2 testing is performed with a field of 3V/m, which is classified by the test standard as a "moderate electromagnetic radiation environment." Level 3 testing is performed with a field of 10V/m, which is classified by the standard as a "severe electromagnetic radiation environment."

EN 61000-4-4 Burst testing is performed on a non-conducting table, with 1 meter of the network cable clamped in a high-voltage burst generation apparatus. Under the test, proper operation continues with occasional loss of a packet. There are three bursts injected onto the network cable each second. Level 3 testing is performed with ±1kV bursts, which are classified by the test standard as representative of a "typical industrial environment." Level 4 testing is performed with ±2kV bursts, which are representative of a "severe industrial environment."

EN 61000-4-5 Surge testing is performed on a non-conducting table using specialized surge generation equipment. The surges are injected directly into the network wiring via a coupling circuit. See figure 10 of EN 61000-4-5 (formerly figure 11 of IEC 801-5). Under the test, proper operation continues with the occasional loss of a packet. Level 2 testing is performed with up to ±1kV surges, and Level 3 testing is performed with up to ±2kV surges.

For more information on levels and installation classes, see EN 61000-4-5. The applicable surge test levels and coupling mode specified by EN 61000-4-5 can be found in table A.1 of that specification, as follows:

- balanced circuits/lines;
- coupling mode is line-to-ground, either polarity, the surge waveform is not applied differentially;
- surge waveform is from a 1.2µs /50µs open circuit and (8µs/20µs) short circuit Combination Wave Generator (CWG)for classes 1-4.

EN 61000-4-6 Conducted RF Immunity testing is performed on a metal test table using an RF signal generator, an RF power amplifier, and specialized "coupling-decoupling" network (CDN) devices. A typical test setup for use with LONWORKS network devices is shown in figure 6.4. The test equipment drives a large common-mode noise voltage onto the twisted pair cable that connects to the Equipment Under Test (EUT). The Auxiliary Equipment (AE) must be able to continue communicating with the EUT during the test. The CRC error rate for this communication should generally be less than 1%, indicating a negligible loss of network functionality. During the test, the RF signal generator is set to an amplitude modulation (AM) depth of 80%, and the frequency is slowly swept from 150kHz to 80MHz. Level 2 testing, which represents a "light industrial environment," is performed with an injected common-mode voltage on the EUT's network cable of 3Vrms (15.3Vp-p including

the 80% AM). Level 3 testing, which represents a "harsh industrial environment," is performed with an injected common-mode voltage on the EUT's network cable of 10Vrms (50.9Vp-p including the 80% AM).

Note that the CDN test method is the preferred method according to the EN 61000-4-6 specification. The T2 and S2 CDN models shown in the figures allow LPT-11 network communications to pass through them with negligible signal degradation. Echelon recommends using these CDNs for EN 61000-4-6 testing of LPT-11 transceiver-based devices, rather than using the alternate "Bulk Current Injection" (BCI) technique.

A typical set-up for EN 61000-4-6 testing of an LPT-11-based device and unshielded twisted pair network wire is shown in figure 6.4.

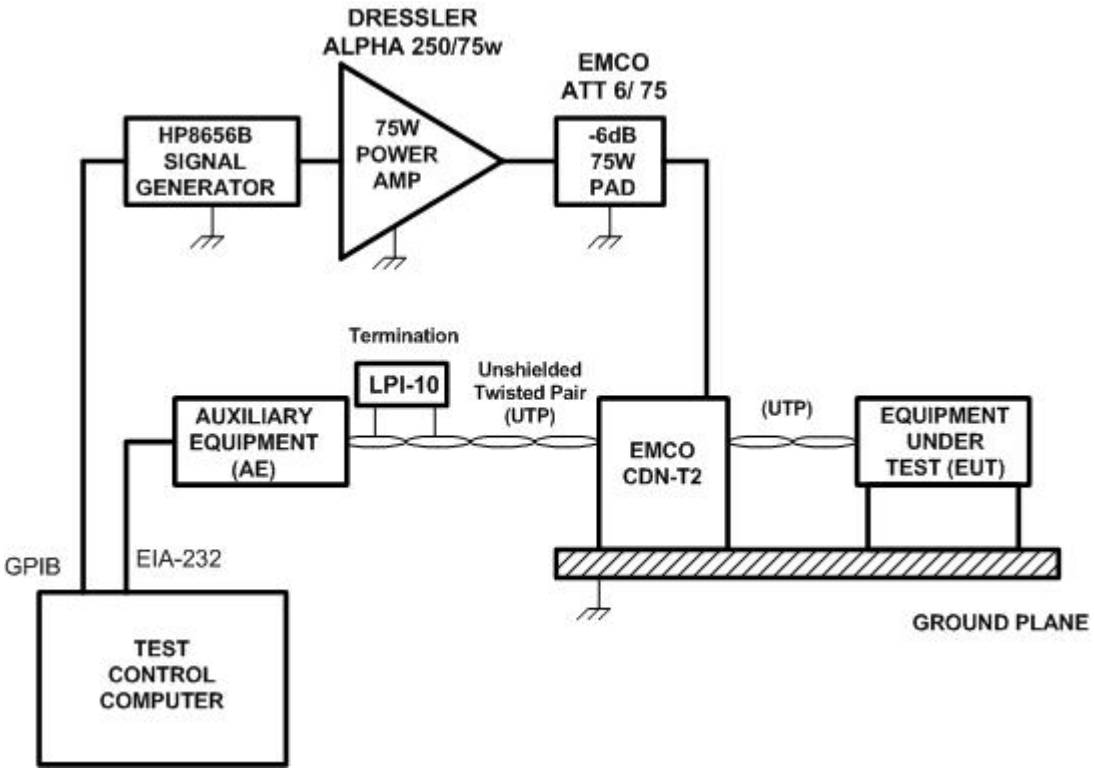


Figure 6.4 Typical EN 61000-4-6 Test Set-up for Unshielded Twisted Pair (UTP)

For the EN 61000-4-6 tests, the EUT is placed on a 10cm high, non-conducting support on top of the metal ground plane. If the EUT's chassis is connected to earth ground in typical installations, then it should be connected directly to the metal ground plane during the EN 61000-4-6 tests via a short wire. If the EUT is left floating in normal use, then there should be no connection between the EUT and earth ground for the EN 61000-4-6 tests. The power is supplied by an LPI-10 source coupler, placed on the AE side of the CDN. During the network immunity tests, any I/O lines that come out of the EUT should also pass through a decoupling network.

The objective of the T2 CDN in the figure is to drive the large common-mode noise signal into the EUT's network cable, while still isolating the AE unit's network cable from the noise. See the EN 61000-4-6 test standard and related articles for more information about test setups and procedures.

The following figure shows the changes in the EN 61000-4-6 test setup to accommodate shielded twisted pair (STP) networks. An S2 CDN is used instead of the T2 CDN, and the shield should be connected to earth ground.

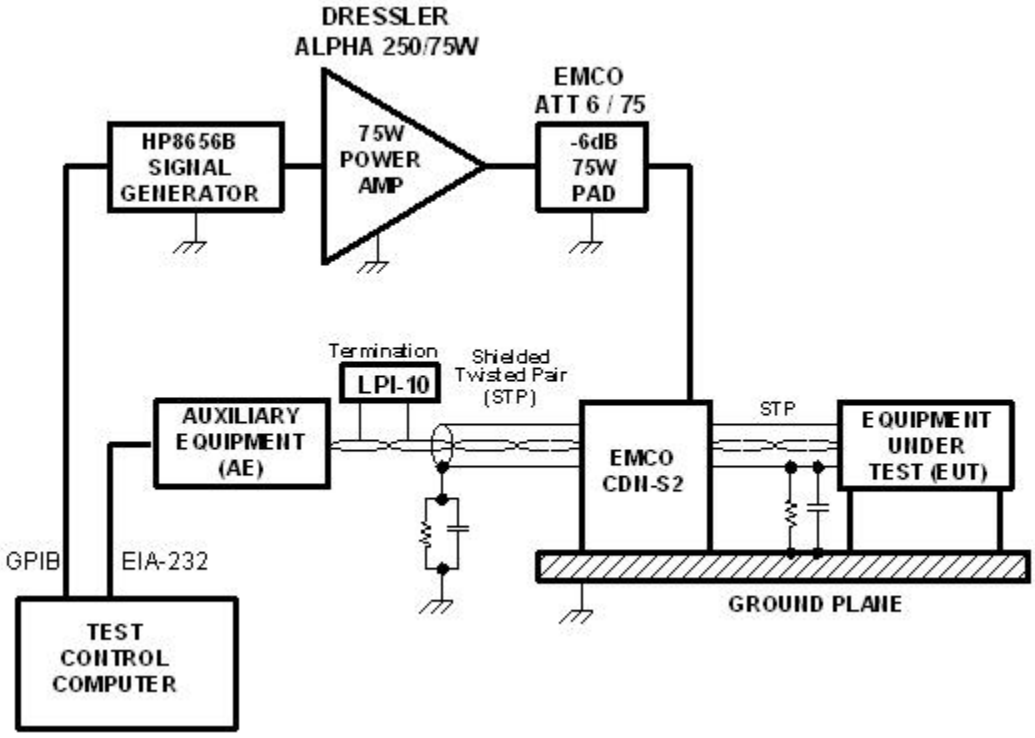


Figure 6.5 Typical EN 61000-4-6 Test Set-up for Shielded Twisted Pair (STP)

Figure 6.6 shows the EN 61000-4-6 common-mode (CM) noise immunity of the LPT-11 transceiver in a typical device during a 15Vrms scan using unshielded twisted pair. The LPT-11 transceiver-based device passes the 10Vrms EN-61000-4-6 Level 3 scan with good margin. For comparison, the CM noise immunity of the LPT-10 transceiver is also plotted in the figure. The CM noise immunity of the LPT-11 transceiver is significantly better than the LPT-10 transceiver.

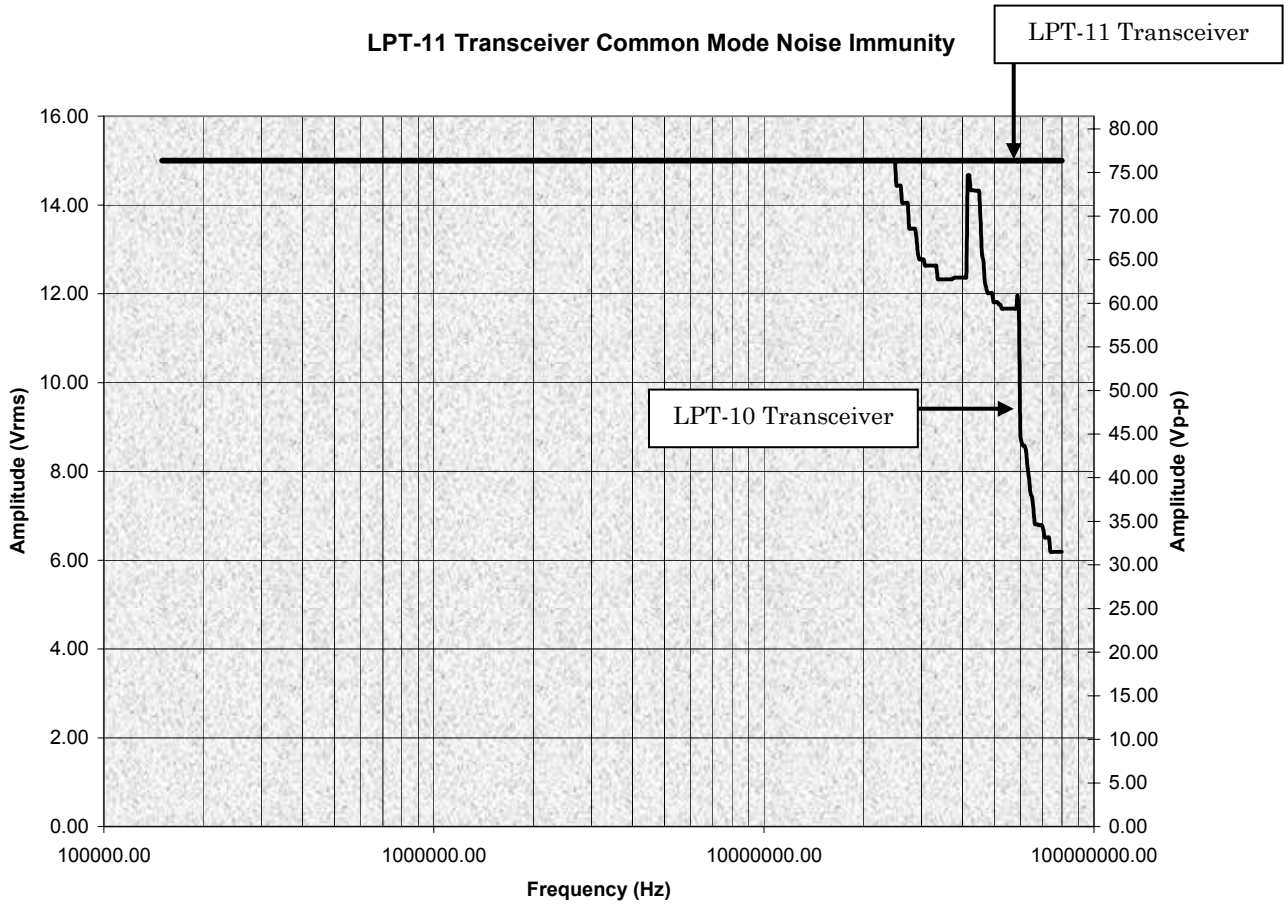


Figure 6.6 LPT-11 Common-Mode Noise Immunity

7
Programming Considerations

This section explains the integration of the LPT-11 Link Power Transceiver using the LonBuilder Developer's Workbench and NodeBuilder Development Tool. It covers considerations relating to channel definition and custom device image generation.

Application Program Development and Export

Applications are initially developed, tested, and debugged using the LonBuilder Developer's Kit or the NodeBuilder Development Tool. See the *LonBuilder User's Guide* or the *NodeBuilder User's Guide* for detailed instructions on developing and testing applications. For updates to the development procedures, also see the ReadMe.txt file installed by the latest service pack for the development tool. Actual unit and system testing of an application targeted for an LPT-11-based device requires one or more Echelon Model 77040 FTM-10 SMX™ Standard Modular Transceivers combined with an Echelon Model 25000 Neuron Emulator inside of a LonBuilder Development Station, or an Echelon Model 65150-24P LTM-10A/FT-10 Platform. The following two sections describe specifics related to each development environment.

LonBuilder Developer's Workbench

Development Hardware Setup

When developing a device that uses an LPT-11 transceiver, the ideal development environment connects all LonBuilder Neuron Emulators to a single TP/FT-10 twisted pair channel to enable system test and protocol analysis of the functioning control network. An FTM-10 transceiver attaches to each of the LonBuilder Neuron Emulators using the Echelon Model 27100 SMX Adapter mounted on the transceiver expansion connectors. Refer to the *LonBuilder Hardware Guide* and *LONWORKS SMX Transceiver Installation Instructions* for detailed instructions on installing the SMX adapter and FTM-10 transceiver.

Warning: A common mistake is to forget to reposition the backplane transceiver jumpers on the LonBuilder Emulator to the *External Transceiver* setting prior to installing the SMX adapter. Also, confirm jumper settings for the FTM-10 transceiver prior to installing on the SMX adapter.

When building an application for a device using an LPT-11 transceiver, the LonBuilder communications port settings must use the standard TP/FT-10 definition. If this is not done prior to building the project, the resulting application will be incompatible with the release hardware. The first step in defining the communications port settings for a device is to create a new channel definition for TP/FT-10, which is accessed by clicking the **Network** button and then the **Channel** button in the LonBuilder Navigator. Create a channel definition which uses **TP/FT-10** as the **Std Xcvr Type** with **Enforce Std Type** set to **Yes**. Versions of the LonBuilder tool prior to Release 3.01 Service Pack 2 do not include the standard transceiver definition for TP/FT-10. Details of the standard transceiver definition are listed in table 7.1 .

Table 7.1 Standard TP/FT-10 Channel Definition for Bus and Free Topologies

Variable	TP/FT-10 Standard Transceiver Type
Comm Mode	Single-ended (see note 4)
Comm Rate	78.13kbps
Min Clock Rate	5MHz
Num Priorities	4

Osc Accuracy	200ppm
Osc Wakeup	0µsec
Avg Packet Size	15 bytes
Collision Detect	No
CD terminate after preamble	No
CD through packet end	No
Bit Sync Threshold	4.0 bits
Rcv Start Delay	9.0 bits (see notes 1 and 2)
Rcv End Delay	0.0 bits
Indeterm Time	24.0 bits
Min Interpacket Time	0.0 bits
Turnaround	0 µsec
Missed Pream	4.0 bits (see notes 1 and 3)
Use Raw Data?	No

Note 1) For the following, "N" must be 1 for the interoperable LONMARK TP/FT-10 channel type.

Note 2) For N repeaters in a packet path: Rcv Start Delay = 4.5 * (N + 1) bits.

Note 3) For N repeaters in a packet path: Missed Pream = 2.0 * (N + 1) bits.

Note 4) Use differential mode when emulating a TP/FT-10 channel on the LonBuilder backplane.

As an alternative to using FTM-10 transceivers, the backplane in the LonBuilder Development Station can approximate the network performance of an LPT-11 transceiver. This is accomplished by creating a channel with TP/FT-10 selected as the transceiver type, setting **Enforce Std Type** to **No** and changing the **Comm Mode** type to **Differential**.

Once the TP/FT-10 channel definition has been created, the hardware definition for the target platform must be defined. During development, the LonBuilder Emulator can can be used to emulate the memory map of the target hardware. To define a hardware template click the **App Node** button and then the **Properties** button from the LonBuilder Navigator. Table 7.2 lists the hardware properties for a typical device using an LPT-11 transceiver.

Table 7.2. Typical LonBuilder Hardware Template Values for a Device Using an LPT-11 Transceiver

HW Property Name	**Value**
Neuron Chip	3150
Input Clock Rate	10MHz
ROM Size	0
Flash Size	128 pages
RAM Size	0

The final step in the process is the selection of a target hardware platform. In the development phase, a LonBuilder Emulator is used. To select this target hardware, click the **App Node** button and then the **Target HW** button from the LonBuilder Navigator. Create a target hardware template that uses **Emulator** as the **HW Type**, the TP/FT-10 channel definition created earlier (described above) as the **Channel Name**, and the hardware template created earlier (described above) as the **HW Prop. Name**.

The LonBuilder environment is now ready for application code to be written, built, and loaded on the development platform.

Release Hardware Setup

The only difference between the development hardware setup and the release hardware setup is the selection of the target hardware in the final step. The channel definition and hardware template used in the development hardware setup may be used to build the release version of the application.

The change to the target hardware step is not a requirement, because the programmable application image file (.nxe extension) from the development build can be used to program the target hardware. However, for target hardware designs that use flash memory to store the application, the LonBuilder tool can load the application image over the network.

To select the release hardware as a target for a build, click the **App Node** button and then the **Target HW** button from the LonBuilder Navigator. Create a target hardware template that uses **Custom Node** as the **HW Type**, the TP/FT-10 channel definition created earlier (described above) as the **Channel Name**, and the hardware template created earlier (described above) as the **HW Prop. Name**.

Refer to the *Building Custom Node* section of Chapter 7 of the *LonBuilder User's Guide* for a description of how to migrate the application from LonBuilder Emulators to production hardware.

Warning: In custom designs using flash memory, the programmed device must be explicitly secured by the PROM programmer once the image is programmed. See Software Data Protection (SDP) information provided by the manufacturer of the PROM programmer.

NodeBuilder Development Tool

The NodeBuilder Development Tool, Release 3 and newer, manages two application and target hardware configurations for each project. One is the *development target* and the other is the *release target*. Development targets are used during development; release targets are used when development is complete and the device is ready for release to production.

Development Hardware Setup

Application development for a device using an LPT-11 transceiver is typically performed using an LTM-10A/FT-10 Platform. Using this platform allows you to develop and test your device application before your target hardware is available. This platform includes a Neuron Chip with a 32KB RAM that can be used for running and debugging your application. To use the LTM-10A/FT-10 Platform during development, define a development target with an LTM-10A RAM hardware template, and specify TP/FT-10 as the transceiver type. You can select the LTM-10A RAM device template using the NodeBuilder Device Template Wizard, or you can select it by dragging the LTM-10A RAM icon from the Standard Templates folder located in the Hardware Templates folder to the device template Development folder for the device.

To communicate with the LTM-10A platform, the NodeBuilder computer must have an LNS compatible network interface with a TP/FT-10 transceiver. Alternatively, you can use a router between the NodeBuilder computer and the LTM-10A platform if they use incompatible transceivers.

The LTM-10A platform has a 10MHz input clock. If the release hardware uses a different input clock rate, the design of the application must be tolerant of the changed execution performance.

Release Hardware Setup

To build an application image for your production hardware, define a release target that specifies a TP/FT-10 transceiver, and that specifies the memory map and Neuron Chip configuration used by your production hardware. Refer the *NodeBuilder User's Guide* and follow the steps listed in this section, to define the release target.

If the final target device does not match the stardard hardware templates, create a user hardware template. You can copy a standard hardware template by dragging it to the User Templates folder in the Hardware Templates folder of the Project pane and then edit the copy, or you can create a new user hardware template.

1 Enter a name for your new hardware template and modify the hardware template properties as follows: Specify the target hardware clock speed in **Clock Speed** on the Hardware tab.

2 Specify the address map on the Off-chip Memory tab for the device. For example, a 32K part will have **Non-volatile End** set to 7FFF and all other fields set to 0.

3 Select the memory part **Type**.

4 For flash memory parts, specify the sector size. For EEPROM memory, set the write time. A list of Echelon tested external memory components can be found on the Echelon website at www.echelon.com.

Once the hardware template has been created, drag the new hardware template to the release target. To do this, drag the newly created icon in the User Templates folder to the Release folder of the device template to complete the procedure.

You can update the user hardware template at any time by double-clicking the template icon and entering the changes. Your new changes will affect any projects opened and compiled using this template. A Build All may be required if you change a hardware template without making any other changes.

Warning: Flash memory must be explicitly secured by the PROM programmer once the image is programmed. See SDP information provided by the manufacturer of the PROM programmer.

8

References

This section provides a list of the reference material used in the preparation of this manual.

Reference Documentation

The documentation used in this manual was from the following sources.

Echelon Documents

LONWORKS LPI-10 Link Power Interface Module User's Guide, Echelon Corporation, part number 078-0104-01.

Toshiba TMPN3150 Neuron Chip data book, part number BPL9 99 805.

LONWORKS Custom Node Development engineering bulletin, Echelon Corporation, 1992, part number 005-0024-01.

LONWORKS FTT-10A Free Topology Transceiver User's Guide, Echelon Corporation, part number 078-0156-01.

Junction Box and Wiring Guidelines for Twisted Pair LONWORKS Networks, Echelon Corporation, part number 005-0023-01.

Textbook References

Protection of Electronic Circuits from Overvoltages, by Ronald B. Standler, John Wiley & Sons, 1989.

EMC Documents

FCC Part 15 Subpart B Class B Using:
    CISPR 22, 1997, Class B
    ANSI C63.4 (1992)method
EN 55024, 1998
EN 61000-4-2, 1995, Electrostatic Discharge
EN 61000-4-3, 1997, Radiated Immunity
EN 61000-4-4, 1995, Electrical Fast Transient Burst
EN 61000-4-5, 1995, Surge
EN 61000-4-6, 1996, Conducted Immunity
EN 61000-4-8, 1994, Magnetic Immunity
EN 55022, 1998, Class B, Radiated Emission
EN 50065-1, 1999, Class B, Conducted Emission

Safety Documents

UL 60950, 2000, Safety for Information Technology Equipment (USA)
CSA C22.2 #60950, 2000, Safety for Information Technology Equipment (Canada)
EN 60950, 2000, Safety for Information Technology Equipment (European Union)

Appendix A

Physical Layer Repeaters

This section explains the physical layer repeater function of the LPT-11 transceiver.

Physical Layer Repeaters

Each link power transceiver incorporates a physical layer repeater function. If a link power system grows beyond the maximum number of transceivers or total wire length, then additional link power systems can be added by interconnecting transceivers using the physical layer repeater function (figure A.1). The physical layer repeater will transfer all LonTalk packets between the two segments, potentially doubling the number of transceivers as well as the total length of wire over which they communicate. The physical layer repeater function permits a link power system to grow as system needs expand, without retrofitting existing controllers or requiring the use of specialized bridges. Note that systems requiring high levels of network traffic may benefit from the use of LONWORKS routers, which forward packets only when necessary. LONMARK Interoperability requires that there be a maximum of one repeater between any two LPT-11 or FTT-10A devices.

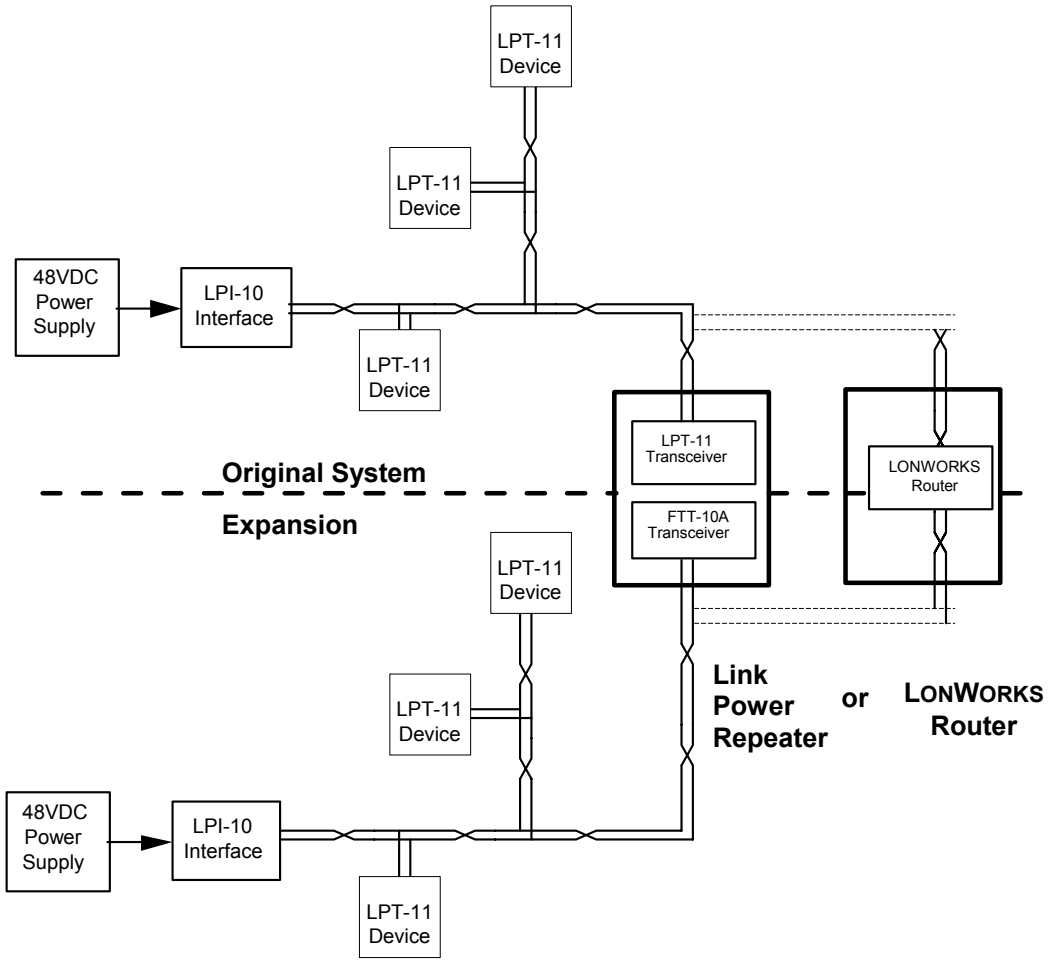


Figure A.1 Link Power Repeater and Router Options for System Expansion

If the limits on the number of transceivers or total wire distance are exceeded, then a link power physical layer repeater (figure A.2) can be added to interconnect two link power network segments, or to connect a link power segment to other non-powered FT segments.

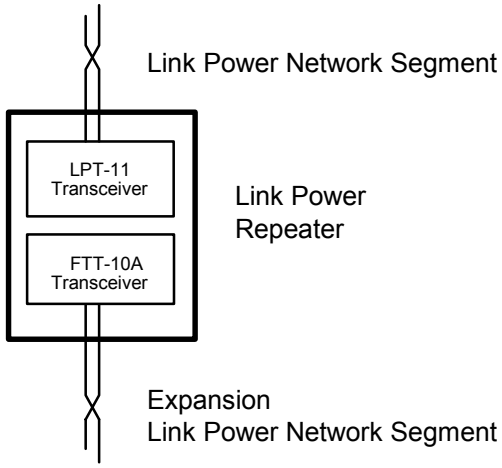


Figure A.2 Two-Way Physical Layer Repeater Block Diagram

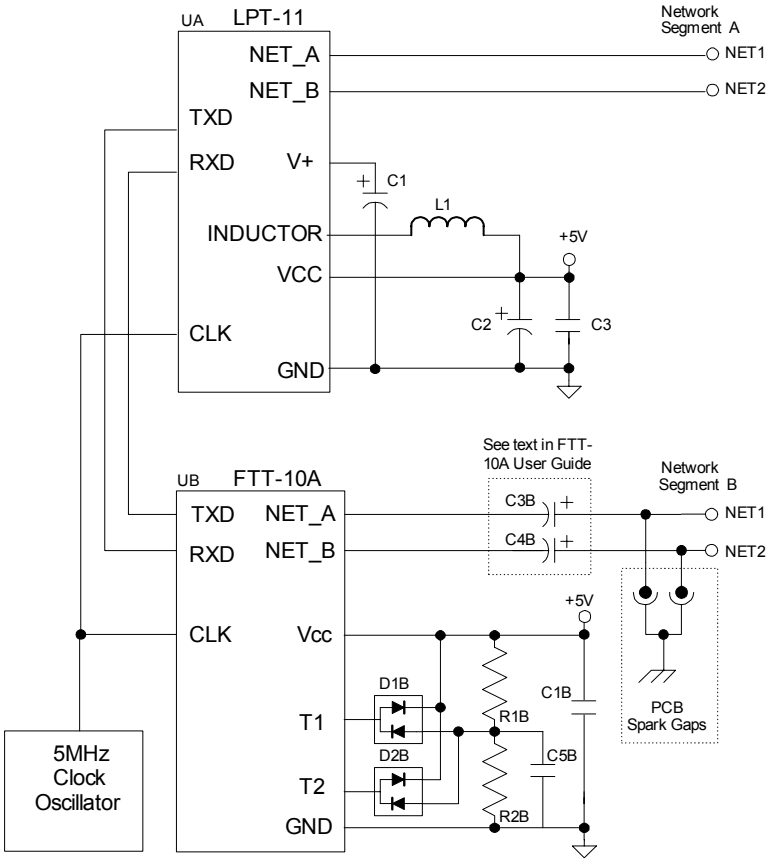
The LPT-11 transceiver is configured as a physical layer repeater by connecting it "back-to-back" with one or more FTT-10A transceivers as shown in the following figures. Only one LPT-11 transceiver may be used in a physical layer repeater – the other transceiver(s) must be an FTT-10A transceiver.

Figure A.3 shows the schematic for a two-way physical layer repeater that operates from 0°C to +85°C. Figure A.4 shows an N-way physical layer repeater that operates from 0°C to +85°C, where N can be from three to four. Figure A.5 shows an N-way physical layer repeater that operates from -40°C to +85°C, where N can be from two to four. The LPT-11 SIP supplies the operating current for the FTT-10A transceivers, the oscillator, and any other circuitry in the physical layer repeater. Note that a toroidal or shielded inductor may be needed for the L1 inductor in the LPT-11 DC-DC converter circuit in physical layer repeaters. Please see Appendix D of the *FTT-10A Free Topology Transceiver User's Guide* for more information.

A packet that is received on any network segment is retransmitted on the other segment(s). The physical layer repeater derives its operating power from the link power network segment that is connected to the LPT-11 transceiver. See the *FTT-10A Free Topology Transceiver User's Guide* for more information about physical layer repeaters built using the FTT-10A transceiver. Information about the JEDEC programming file for the 22V10 PAL that is shown in figure A.5 can also be found in the *FTT-10A Free Topology Transceiver User's Guide*.

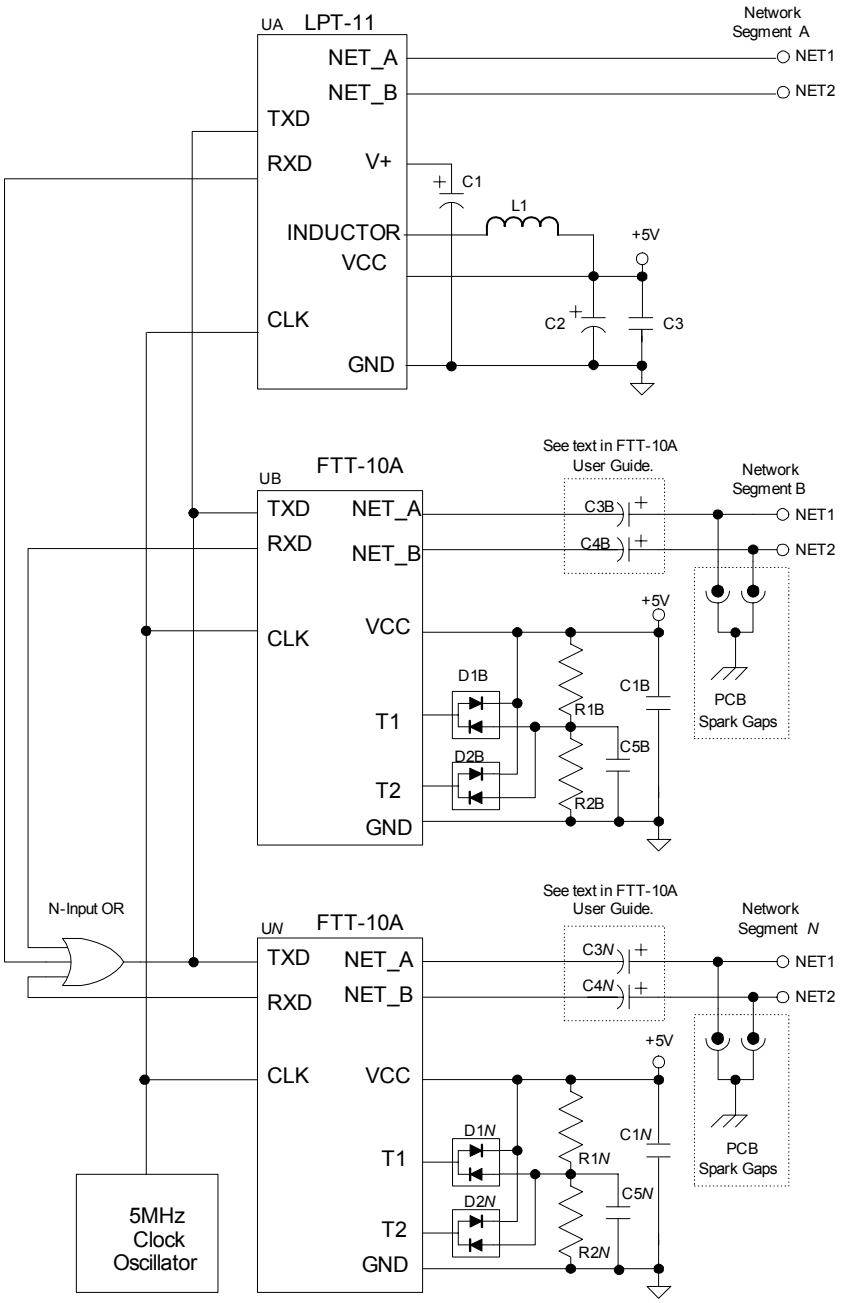
The maximum Idd that can be drawn from the LPT-11 SIP is 100mA, so the total of the current consumption of the FTT-10A transceivers, plus the current consumption of the oscillator and any other circuitry must be less than or equal to 100mA maximum. This limits the total number of segments for an LPT-11 SIP-based physical layer repeater to five or less, since each FTT-10A transceiver draws 20mA maximum when in transmit mode. When the LPT-11 transceiver is receiving a

packet, all of the FTT-10A transceivers in the physical layer repeater will be in transmit mode, repeating the packet onto their respective segments. Therefore, in a 5-way physical layer repeater, the maximum current consumption when the LPT-11 transceiver is in receive mode is 4 x 20mA = 80mA, plus the current consumption of the oscillator and other logic.



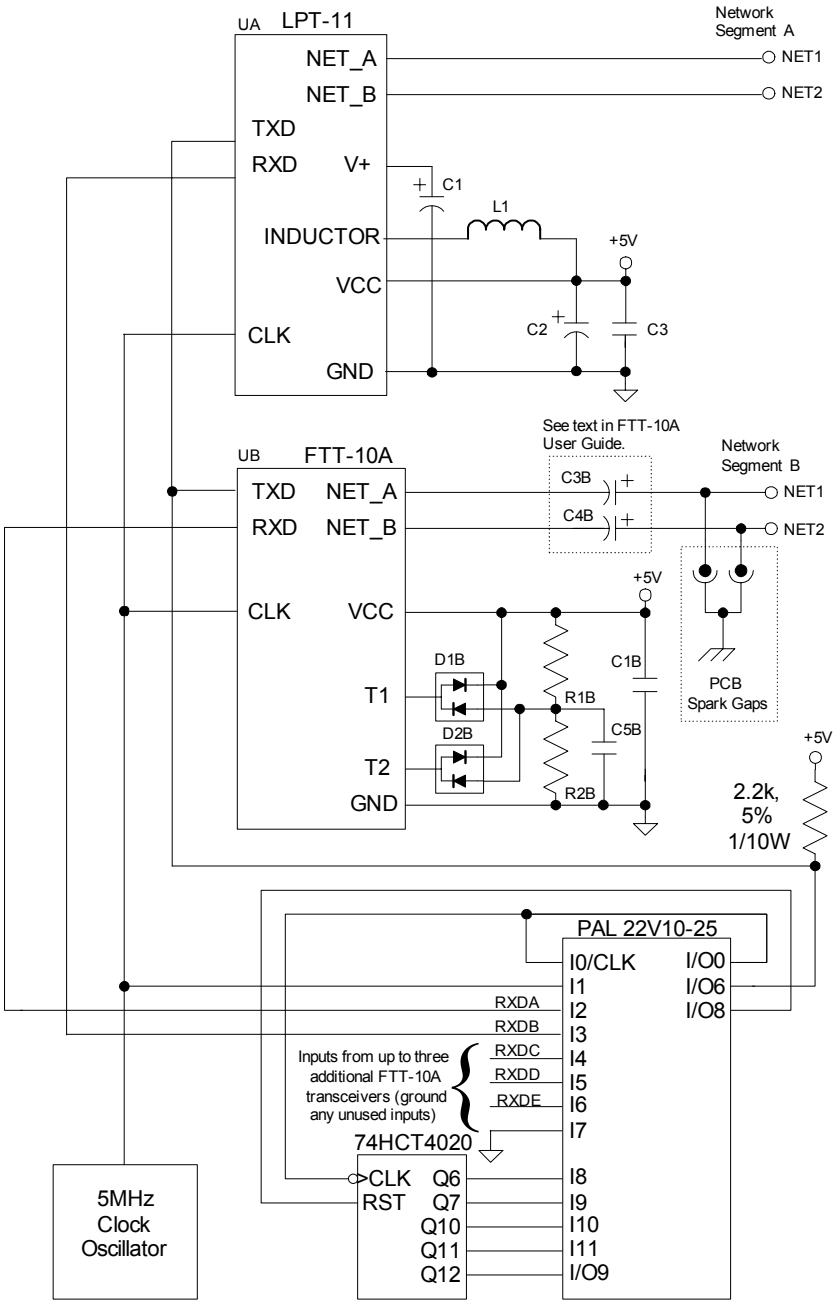
R1B 1500Ω, 1%, 1/10W
R2B 576Ω, 1%, 1/10W
C1B 0.1 µF
C3B 22µF, +50V polar (see *FTT-10A Free Topology Transceiver User's Guide)*.
C4B 22µF, +50V polar (see *FTT-10A Free Topology Transceiver User's Guide)*.
C5B 0.1 µF, X7R or Y5V ceramic
Note that a toroidal or shielded inductor should be used for L1 on all physical layer repeaters.
See Chapter 2 for LPT-11 transceiver component values L1 and C1, C2, C3.
Other components per table 2.3 in *FTT-10A Free Topology Transceiver User's Guide*.

Figure A.3 Two-Way Physical Layer Repeater Schematic
(0°C to +85°C)



R1B 1500Ω, 1%, 1/10W
R2B 576Ω, 1%, 1/10W
C1B 0.1 µF
C3B 22µF, +50V polar (see *FTT-10A Free Topology Transceiver User's Guide)*.
C4B 22µF, +50V polar (see *FTT-10A Free Topology Transceiver User's Guide)*.
C5B 0.1 µF, X7R or Y5V ceramic
Note that a toroidal or shielded inductor should be used for L1 on all physical layer repeaters.
See Chapter 2 for LPT-11 transceiver component values L1 and C1, C2, C3.
Other components per table 2.3 in *FTT-10A Free Topology Transceiver User's Guide*.

Figure A.4 N-Way Physical Layer Repeater Schematic (0°C to +85°C), For N = 3 to 5



R1B 1500Ω, 1%, 1/10W
R2B 576Ω, 1%, 1/10W
C1B 0.1 µF
C3B 22µF, +50V polar (see *FTT-10A Free Topology Transceiver User's Guide).*
C4B 22µF, +50V polar (see *FTT-10A Free Topology Transceiver User's Guide).*
C5B 0.1 µF, X7R or Y5V ceramic
Note that a toroidal or shielded inductor should be used for L1 on all physical layer repeaters.
See Chapter 2 for LPT-11 transceiver component values L1 and C1, C2, C3.
Add power supply bypass capacitors (not shown) next to oscillator, 74HCT4020 and PAL.
PAL requires programming. See the *FTT-10A Free Topology Transceiver User's Guide.*
Other components per table 2.3 in *FTT-10A Free Topology Transceiver User's Guide.*

Figure A.5 N-Way Physical Layer Repeater Schematic
(-40°C to +85°C), For N = 2 to 5

Appendix B

Differences Between LPT-10 and LPT-11

This appendix contains information on differences in design from the LPT-10 to the LPT-11 transceiver.

Differences between LPT-10 and LPT-11 Link Power Transceivers

The following sections discuss the functional differences between the LPT-10 and LPT-11 transceivers, as well as differences in form, plus address the modifications required for migrating from the LPT-10 to the LPT-11.

Functional Differences

The LPT-11 transceiver is approximately 10 times more immune to high frequency common mode noise than the LPT-10. The LPT-11 transceiver can operate reliably in the presence of 10Vrms common mode noise. This enables properly designed devices to meet the European EN 61000-4-6 Level 3 specifications.

The LPT-11 transceiver does not support a Wake-Up Timer feature. The wake-up timer was provided to "wake" the Neuron Chip from SLEEP mode periodically to sample inputs/outputs and communicate with the network.

Note: If there are designs in which LEDs have been connected to TXEN/RX_ACTIVE pins, such an implementation will no longer be feasible. This implementation was not previously supported by Echelon.

The LPT-11 transceiver does not support operation at 1.25MHz.

The LPT-11 transceiver supports operation at 20MHz.

Differences In Form

The LPT-11 transceiver has 2 less pins than the LPT-10: 14 pins on the LPT-11 transceiver versus 16 pins on the LPT-10 transceiver. The 2 pins that have been eliminated are # 15 WAKEUP-OUT and #16 RX_ACTIVE

The WAKEUP-OUT pin on the LPT-10 transceiver was eliminated since the wake up timer feature is no longer supported. The RX_ACTIVE pin is no longer needed since a physical layer repeater configuration can now be supported without the need for RX_ACTIVE.

Certain other pins have been designated No Connect (NC) pins, i.e., these pins are not connected internally. The newly designated NC pins should not affect existing LPT-10 transceiver designs when they migrate to the LPT-11 transceiver. Pin changes are as follows:

- Pin # 8 CLKSEL0 becomes a NC.
- Pin # 9 TXD/CLKSEL1 becomes TXD.

- In the LPT-10 transceiver the CLKSEL0 and the CLKSEL1 pins are used to select the frequency of the input clock. The new LPT-11 transceiver design has an auto clock select feature and does not require the functionality previously provided by the CLKSEL0 and the CLKSEL1 pins.
- Pin #11 TXEN becomes NC. In the LPT-10 transceiver the TXEN pin is connected to the CP2 of the Neuron Chip to indicate to the transceiver that Neuron Chip is transmitting packets. This fuctionality is no longer required in the LPT-11 transceiver.
- Pin #12 ~RESET becomes NC. In the LPT-10 transceiver this pin is connected to the RESET pin of the Neuron Chip. In the LPT-11 transceiver, the Neuron Chip RESET is detected by the CP1 pin going to high impedance.
- Pin #13~SLEEP becomes NC. In the LPT-10 transceiver this pin was connected to the CP3 pin on the Neuron Chip to put LPT-10 transceiver into the sleep mode. This functionality is no longer required in the LPT-11 transceiver since the SLEEP mode is not supported by the LPT-11 transceiver.
- Pin #14 WAKEUP-CAP becomes NC. In the LPT-10 transceiver the WAKEUP-CAP pin was used to set the frequency of the Wake-Up Timer. This functionality is no longer needed since wake up timer is not supported on the LPT-11 transceiver.

The LPT-11 transceiver SIP does not have the outer phenolic coating that the LPT-10 transceiver SIP has.

The LPT-11 transceiver SIP is slightly smaller than the LPT-10. Dimensions in mm are shown in the following table, with inches in parentheses.

	LPT-11 Transceiver	**LPT-10 Transceiver**
Height	19.80 (0.780)	19.80 (0.780)
Width	28.50 (1.122)	31.50 (1.240)
Thickness	4.15 (0.163)	8.00 (0.315)
Pin Height	5.5 ±0.5 (0.22 ± 0.02)	7.0 (0.276)

Modifications for Migrating from the LPT-10 to the LPT-11 Transceiver

The 47k Ohm resistor on Pin #9 (TXD/CLKSEL1 on the LPT-10 transceiver) should be removed.

Appendix C

LPT-11 Transceiver-Based Device Checklist

This appendix includes a checklist to ensure that products using the LPT-11 transceiver meet the specifications presented in this user's guide.

LPT-11 Transceiver-based Device Checklist

LPT-11 Transceiver and Neuron Chip Connections

Item	*Check When Completed*	*Description*
1		Transceiver pins connected as shown in table 2.1 and figure 2.1
2		The recommended number and placement of 0.1µF bypass capacitors are near the Neuron Chip. See the appropriate Neuron Chip Databook from Toshiba or Cypress, or the FT 31xx Smart Transceiver Databook from Echelon, as appropriate. *Note: No more than 1.0µF of total decoupling capacitance can be connected to Vcc.*
3		The Neuron Chip and transceiver input clock frequency is ≥5MHz and accurate to at least ±200ppm for compatibility with the LONMARK TP/FT-10 channel. Use of a 2.5MHz clock frequency is possible with the LPT-11 transceiver, but it is not compatible with the LONMARK TP/FT-10 channel.
4		If required, a Low Voltage Interrupt (LVI) circuit with open collector output (such as the Motorola MC33064) is used to supply a reset signal to the Neuron Chip. See the appropriate *Neuron Chip Databook* for details on when an LVI is needed.

LPT-11 PCB Layout

Item	*Check When Completed*	*Description*
5		The network connector, LPT-11 Transceiver SIP, and DC-DC converter components L1, C1, and C2 are placed close together, following the general layout guidelines of figure 2.2.
6		The traces that carry moderate DC-DC switching currents are wide and short (the V+ and INDUCTOR nets).
7		The Neuron Chip and transceiver SIP are placed adjacent to one another on the same PCB, following the general layout guidelines of figure 2.2.
8		CLK2 from Neuron Chip is connected to the SIP's CLK pin via a trace that is ≤ 2cm (0.8") long.

9		The CLK2 trace from the Neuron Chip to the transceiver is guarded by ground.
10		The LPT-11 device's logic ground is electrically floating from all external ground connections.
11		The “leakage” capacitance the LPT-11 device's logic ground to external ground is minimized, preferably less than 10pF.
12		The PCB has a 14-hole pattern for the SIP, according to the mechanical dimensions in figure 3.1. If the LPT-11 SIP is being loaded into a PCB that still has the LPT-10 SIP's 16-hole pattern, appropriate assembly instructions are in place to ensure that the 14-pin LPT-11 SIP is loaded with its pin-1 in the pin-1 hole of the LPT-10 pattern.

LPT-11 DC-DC Converter

Item	***Check When Completed***	***Description***
13		The DC-DC switching inductor L1 meets the following criteria over the device's operating temperature range: L=1mH ± 10%, Isat≥200mA, and DCR ≤ 4 Ω.
14		The DC-DC input storage capacitor C1 meets the following criteria over the device's operating temperature range: C=100µF ±20%, DCWV ≥ 63V, Iripple ≥ 200mArms @ 100kHz, ESR ≤ 1.2Ω @100kHz.
15		The DC-DC output capacitor C2 meets the following criteria over the device's operating temperature range: C=22µF ±20%, DCWV ≥ 10V, Iripple≥ 200mArms@100kHz, ESR ≤ 1.2Ω @100kHz.
16		For applications that require no more than 25mA of sustained peak Icc application current, L1, C1, and C2 meet at least the relaxed specifications presented in table 2.6.
17		In addition to the 22µF capacitor C2, no more than 1.0µF of decoupling capacitance has been added to Vcc.
18		The lifetimes of C1 and C2 have been calculated, and an appropriate capacitor vendor and series has been chosed to meet the product’s expected operational lifetime.
19		If a periodic load is connected to Icc in this device with a load frequency in the 10kHz to 1MHz range, that load’s Vcc supply is post-filtered, as shown in figure 4.1.
20		If the device’s application circuitry or other nearby circuitry can be disturbed by AC magnetic fields, then a toroidal or shielded inductor is used for L1.

LPT-11 Transient Immunity

Item	*Check When Completed*	*Description*
21		If 1.0kV or 2.0kV surge immunity is desired, an appropriate TVS device from table 6.1 is placed differentially across NET_A and NET_B. For 0.5kV surge immunity, no TVS should be needed.
22		The device's package is designed to prevent ESD hits from arcing into the node's internal circuitry.

LPT-11 Transceiver Programming

Item	*Check When Completed*	*Description*
23		The standard TP/FT-10 channel is defined for the device (for devices with Neuron chip clock rates of ≥ 5MHz only).
24		If the device operates with 2.5MHz Neuron Chip clock, it will not be used on any networks that use the standard TP/FT-10 comm parameters.

Link Power Network Considerations

Item	*Check When Completed*	*Description*
25		The network uses a wire type listed in tables 5.2 and 5.3.
26		The network length obeys the datacomm transmission specifications described in tables 5.2 and 5.3.
27		The network also obeys the power-limited distance specifications described in chapter 5 (either the Simplified Form or the Extended Performance Form).
28		If the network configuration is Free Topology, one LPI-10 Source Coupler is used anywhere in the network to provide power to the network, and the LPI-10 Source Coupler's termination jumper is in the "1CPLR" setting.

29		If the network configuration is Doubly-Terminated Bus, one LPI-10 source coupler is placed at one end of the bus to provide power and one termination (with its termination jumper in the "2CPLR" setting), plus a standard 105Ω TP/FT termination is placed the other end of the DT Bus (see figure 5.6.)

LPT-11 Physical Layer Repeater

Item	*Check When Completed*	*Description*
30		Only one LPT-11 transceiver is used per physical layer repeater. The other 1-4 segments (for 2-way to 5-way physical layer repeaters) connect to the physical layer repeater using FTT-10A transceivers.
31		The LPT-11 transceiver-based physical layer repeater connects to no more that five total segments, and the peak Icc loading is no more than 100mA total.
32		For physical layer repeaters that operate from 0°C to +85°C, a circuit shown in figure A.3 or A.4 is used.
33		For physical layer repeaters that operate below 0°C, the PAL-based circuit shown in figure A.5 is used.
34		The LPT-11 switching inductor L1 is a toroid or a shielded inductor type on the physical layer repeater or else no magnetic field coupling is seen when making the measurements described in Appendix D of the *LONWORKS FTT-10A Free Topology Transceiver User's Guide*, "Avoiding Magnetic Field Interference."
35		For 3-way, 4-way, and 5-way physical layer repeaters, the FTT-10A transceivers are spaced at least 2.5cm (1") apart from one another, as described in the PLR section of the *LONWORKS FTT-10A Free Topology Transceiver User's Guide.*